

### FEATURES

- Operating frequency from 100 MHz to 4000 MHz**
- Digitally controlled VGA with serial and parallel interfaces**
- 6-bit, 0.5 dB digital step attenuator**
- 31.5 dB gain control range with  $\pm 0.25$  dB step accuracy**
- Gain Block Amplifier 1**
  - Gain: 19.2 dB at 2140 MHz**
  - OIP3: 40.2 dBm at 2140 MHz**
  - P1dB: 19.8 dBm at 2140 MHz**
  - Noise figure: 2.9 dB at 2140 MHz**
- 1/4 W Driver Amplifier 2**
  - Gain: 14.2 dB at 2140 MHz**
  - OIP3: 41.1 dBm at 2140 MHz**
  - P1dB: 26.0 dBm at 2140 MHz**
  - Noise figure: 3.7 dB at 2140 MHz**
- Gain block, DSA, or 1/4 W driver amplifier can be first**
- Low quiescent current of 175 mA**
- The companion [ADL5240](#) integrates a gain block with DSA**

### APPLICATIONS

- Wireless infrastructure**
- Automated test equipment**
- RF/IF gain control**

### GENERAL DESCRIPTION

The [ADL5243](#) is a high performance, digitally controlled variable gain amplifier operating from 100 MHz to 4000 MHz. The VGA integrates two high performance amplifiers and a digital step attenuator (DSA). Amplifier 1 (AMP1) is an internally matched gain block amplifier with 20 dB gain, and Amplifier 2 (AMP2) is a broadband 1/4 W driver amplifier. The DSA is 6-bit with a 31.5 dB gain control range, 0.5 dB steps, and  $\pm 0.25$  dB step accuracy. The attenuation of the DSA can be controlled using a serial or parallel interface. The gain block and DSA are internally matched to 50  $\Omega$  at their inputs and outputs, and all three internal devices are separately biased. The separate bias allows all or part of the [ADL5243](#) to be used, which allows for easy reuse throughout a design. The pinout of the [ADL5243](#) also enables the gain block, DSA, or 1/4 W driver amplifier to be first, giving the VGA maximum flexibility in a signal chain.

The [ADL5243](#) consumes 175 mA and operates off a single supply ranging from 4.75 V to 5.25 V. The VGA is packaged in a thermally efficient, 5 mm  $\times$  5 mm, 32-lead LFCSP and is fully specified for operation from  $-40^{\circ}\text{C}$  to  $+85^{\circ}\text{C}$ . A fully populated evaluation board is available.

### FUNCTIONAL BLOCK DIAGRAM

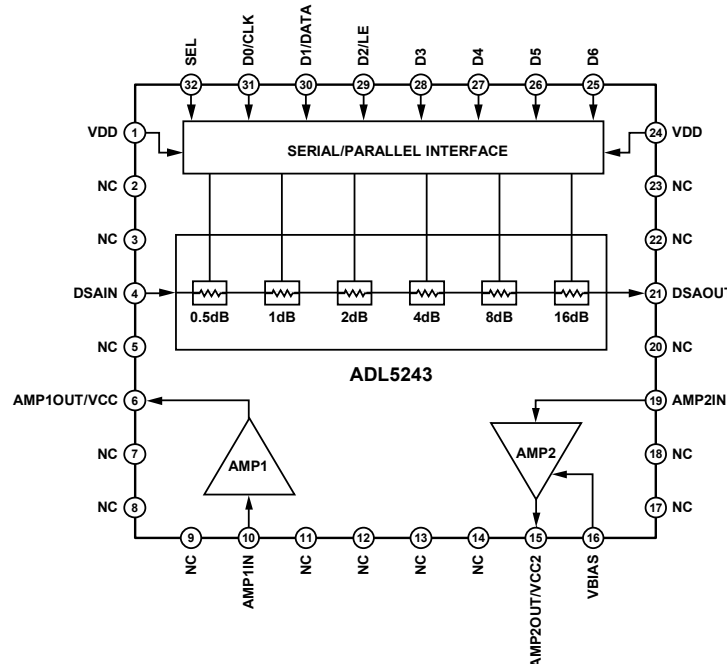


Figure 1.

#### Rev. A

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**REVISION HISTORY**

**8/11—Rev. 0 to Rev. A**

Changes to Features Section.....	1
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**7/11—Revision 0: Initial Version**

## SPECIFICATIONS

VDD = 5V, VCC = 5V, VCC2 = 5V, T<sub>A</sub> = 25°C.

Table 1.

Parameter	Conditions	Min	Typ	Max	Unit
OVERALL FUNCTION					
Frequency Range		100		4000	MHz
AMPLIFIER 1 FREQUENCY = 150 MHz	Using the AMP1IN and AMP1OUT pins				
Gain			18.2		dB
vs. Frequency	±50 MHz		±0.97		dB
vs. Temperature	-40°C ≤ T <sub>A</sub> ≤ +85°C		±0.07		dB
vs. Supply	4.75 V to 5.25 V		±0.03		dB
Input Return Loss	S11		-10.4		dB
Output Return Loss	S22		-8.2		dB
Output 1 dB Compression Point			18.4		dBm
Output Third-Order Intercept	Δf = 1 MHz, P <sub>OUT</sub> = 3 dBm/tone		29.5		dBm
Noise Figure			2.8		dB
AMPLIFIER 1 FREQUENCY = 450 MHz	Using the AMP1IN and AMP1OUT pins				
Gain			20.6		dB
vs. Frequency	±50 MHz		±0.10		dB
vs. Temperature	-40°C ≤ T <sub>A</sub> ≤ +85°C		±0.36		dB
vs. Supply	4.75 V to 5.25 V		±0.01		dB
Input Return Loss	S11		-17.8		dB
Output Return Loss	S22		-16.5		dB
Output 1 dB Compression Point			19.5		dBm
Output Third-Order Intercept	Δf = 1 MHz, P <sub>OUT</sub> = 3 dBm/tone		38.4		dBm
Noise Figure			2.8		dB
AMPLIFIER 1 FREQUENCY = 748 MHz	Using the AMP1IN and AMP1OUT pins				
Gain			20.8		dB
vs. Frequency	±50 MHz		±0.02		dB
vs. Temperature	-40°C ≤ T <sub>A</sub> ≤ +85°C		±0.32		dB
vs. Supply	4.75 V to 5.25 V		±0.01		dB
Input Return Loss	S11		-22.0		dB
Output Return Loss	S22		-21.6		dB
Output 1 dB Compression Point			19.6		dBm
Output Third-Order Intercept	Δf = 1 MHz, P <sub>OUT</sub> = 3 dBm/tone		39.6		dBm
Noise Figure			2.7		dB
AMPLIFIER 1 FREQUENCY = 943 MHz	Using the AMP1IN and AMP1OUT pins				
Gain		19.0	20.3	22.0	dB
vs. Frequency	±18 MHz		±0.01		dB
vs. Temperature	-40°C ≤ T <sub>A</sub> ≤ +85°C		±0.28		dB
vs. Supply	4.75 V to 5.25 V		±0.02		dB
Input Return Loss	S11		-24.0		dB
Output Return Loss	S22		-21.5		dB
Output 1 dB Compression Point		18.5	19.9		dBm
Output Third-Order Intercept	Δf = 1 MHz, P <sub>OUT</sub> = 3 dBm/tone		40.4		dBm
Noise Figure			2.7		dB

Parameter	Conditions	Min	Typ	Max	Unit
<b>AMPLIFIER 1 FREQUENCY = 1960 MHz</b>					
Gain	Using the AMP1IN and AMP1OUT pins		19.5		dB
vs. Frequency	±30 MHz		±0.02		dB
vs. Temperature	−40°C ≤ T <sub>A</sub> ≤ +85°C		±0.26		dB
vs. Supply	4.75 V to 5.25 V		±0.04		dB
Input Return Loss	S11		−13.5		dB
Output Return Loss	S22		−12.4		dB
Output 1 dB Compression Point			19.6		dBm
Output Third-Order Intercept	Δf = 1 MHz, P <sub>OUT</sub> = 3 dBm/tone		40.4		dBm
Noise Figure			2.9		dB
<b>AMPLIFIER 1 FREQUENCY = 2140 MHz</b>					
Gain	Using the AMP1IN and AMP1OUT pins	17.5	19.2	21.5	dB
vs. Frequency	±30 MHz		±0.02		dB
vs. Temperature	−40°C ≤ T <sub>A</sub> ≤ +85°C		±0.26		dB
vs. Supply	4.75 V to 5.25 V		±0.05		dB
Input Return Loss	S11		−13.3		dB
Output Return Loss	S22		−12.2		dB
Output 1 dB Compression Point		17.5	19.8		dBm
Output Third-Order Intercept	Δf = 1 MHz, P <sub>OUT</sub> = 3 dBm/tone		40.2		dBm
Noise Figure			2.9		dB
<b>AMPLIFIER 1 FREQUENCY = 2630 MHz</b>					
Gain	Using the AMP1IN and AMP1OUT pins	17.5	19.0	21.5	dB
vs. Frequency	±60 MHz		±0.03		dB
vs. Temperature	−40°C ≤ T <sub>A</sub> ≤ +85°C		±0.22		dB
vs. Supply	4.75 V to 5.25 V		±0.05		dB
Input Return Loss	S11		−17.3		dB
Output Return Loss	S22		−12.3		dB
Output 1 dB Compression Point		17.5	19.5		dBm
Output Third-Order Intercept	Δf = 1 MHz, P <sub>OUT</sub> = 3 dBm/tone		39.5		dBm
Noise Figure			2.9		dB
<b>AMPLIFIER 1 FREQUENCY = 3600 MHz</b>					
Gain	Using the AMP1IN and AMP1OUT pins		18.0		dB
vs. Frequency	±100 MHz		±0.10		dB
vs. Temperature	−40°C ≤ T <sub>A</sub> ≤ +85°C		±0.05		dB
vs. Supply	4.75 V to 5.25 V		±0.12		dB
Input Return Loss	S11		−30.7		dB
Output Return Loss	S22		−9.0		dB
Output 1 dB Compression Point			18.0		dBm
Output Third-Order Intercept	Δf = 1 MHz, P <sub>OUT</sub> = 3 dBm/tone		34.6		dBm
Noise Figure			3.3		dB
<b>AMPLIFIER 2 FREQUENCY = 748 MHz</b>					
Gain	Using the AMP2IN and AMP2OUT pins		17.5		dB
vs. Frequency	±50 MHz		±0.14		dB
Input Return Loss	S11		−12.7		dB
Output Return Loss	S22		−8.6		dB
Output 1 dB Compression Point			24.7		dBm
Output Third-Order Intercept	Δf = 1 MHz, P <sub>OUT</sub> = 5 dBm/tone		41.5		dBm
Noise Figure			5.6		dB

Parameter	Conditions	Min	Typ	Max	Unit
AMPLIFIER 2 FREQUENCY = 943 MHz	Using the AMP2IN and AMP2OUT pins				
Gain			16.5		dB
vs. Frequency	±18 MHz		±0.05		dB
vs. Temperature	−40°C ≤ T <sub>A</sub> ≤ +85°C		±0.39		dB
vs. Supply	4.75 V to 5.25 V		±0.10		dB
Input Return Loss	S11		−11.2		dB
Output Return Loss	S22		−8.1		dB
Output 1 dB Compression Point			25.0		dBm
Output Third-Order Intercept	Δf = 1 MHz, P <sub>OUT</sub> = 5 dBm/tone		43.3		dBm
Noise Figure			5.3		dB
AMPLIFIER 2 FREQUENCY = 2140 MHz	Using the AMP2IN and AMP2OUT pins	13.0	14.2	15.5	
Gain					dB
vs. Frequency	±30 MHz		±0.03		dB
vs. Temperature	−40°C ≤ T <sub>A</sub> ≤ +85°C		±0.50		dB
vs. Supply	4.75 V to 5.25 V		±0.09		dB
Input Return Loss	S11		−10.7		dB
Output Return Loss	S22		−8.1		dB
Output 1 dB Compression Point			26.0		dBm
Output Third-Order Intercept	Δf = 1 MHz, P <sub>OUT</sub> = 5 dBm/tone		41.1		dBm
Noise Figure			3.7		dB
AMPLIFIER 2 FREQUENCY = 2630 MHz	Using the AMP2IN and AMP2OUT pins				
Gain			13.0		dB
vs. Frequency	±60 MHz		±0.13		dB
vs. Temperature	−40°C ≤ T <sub>A</sub> ≤ +85°C		±0.56		dB
vs. Supply	4.75 V to 5.25 V		±0.09		dB
Input Return Loss	S11		−9.4		dB
Output Return Loss	S22		−8.3		dB
Output 1 dB Compression Point			24.5		dBm
Output Third-Order Intercept	Δf = 1 MHz, P <sub>OUT</sub> = 5 dBm/tone		40.4		dBm
Noise Figure			4.1		dB
DSA FREQUENCY = 150 MHz	Using the DSAIN and DSAOUT pins, minimum attenuation				
Insertion Loss			−1.5		dB
vs. Frequency	±50 MHz		±0.12		dB
vs. Temperature	−40°C ≤ T <sub>A</sub> ≤ +85°C		±0.10		dB
Attenuation Range	Between maximum and minimum attenuation states		28.8		dB
Attenuation Step Error	All attenuation states		±0.18		dB
Attenuation Absolute Error	All attenuation states		±1.35		dB
Input Return Loss			−13.5		dB
Output Return Loss			−13.3		dB
Input Third-Order Intercept	Δf = 1 MHz, P <sub>OUT</sub> = 5 dBm/tone		45.2		dBm

Parameter	Conditions	Min	Typ	Max	Unit
DSA FREQUENCY = 450 MHz	Using the DSAIN and DSAOUT pins, minimum attenuation				
Insertion Loss			-1.4		dB
vs. Frequency	±50 MHz		±0.02		dB
vs. Temperature	-40°C ≤ T <sub>A</sub> ≤ +85°C		±0.12		dB
Attenuation Range	Between maximum and minimum attenuation states		30.7		dB
Attenuation Step Error	All attenuation states		±0.14		dB
Attenuation Absolute Error	All attenuation states		±0.39		dB
Input Return Loss			-17.7		dB
Output Return Loss			-17.4		dB
Input Third-Order Intercept	Δf = 1 MHz, P <sub>OUT</sub> = 5 dBm/tone		41.2		dBm
DSA FREQUENCY = 748 MHz	Using the DSAIN and DSAOUT pins, minimum attenuation				
Insertion Loss			-1.5		dB
vs. Frequency	±50 MHz		±0.02		dB
vs. Temperature	-40°C ≤ T <sub>A</sub> ≤ +85°C		±0.12		dB
Attenuation Range	Between maximum and minimum attenuation states		30.9		dB
Attenuation Step Error	All attenuation states		±0.15		dB
Attenuation Absolute Error	All attenuation states		±0.30		dB
Input Return Loss			-17.1		dB
Output Return Loss			-17.1		dB
Input Third-Order Intercept	Δf = 1 MHz, P <sub>OUT</sub> = 5 dBm/tone		40.4		dBm
DSA FREQUENCY = 943 MHz	Using the DSAIN and DSAOUT pins, minimum attenuation				
Insertion Loss			-1.6		dB
vs. Frequency	±18 MHz		±0.01		dB
vs. Temperature	-40°C ≤ T <sub>A</sub> ≤ +85°C		±0.13		dB
Attenuation Range	Between maximum and minimum attenuation states		30.9		dB
Attenuation Step Error	All attenuation states		±0.15		dB
Attenuation Absolute Error	All attenuation states		±0.28		dB
Input Return Loss			-16.0		dB
Output Return Loss			-15.9		dB
Input 1 dB Compression Point			30.5		dBm
Input Third-Order Intercept	Δf = 1 MHz, P <sub>OUT</sub> = 5 dBm/tone		48.3		dBm
DSA FREQUENCY = 1960 MHz	Using the DSAIN and DSAOUT pins, minimum attenuation				
Insertion Loss			-2.5		dB
vs. Frequency	±30 MHz		±0.04		dB
vs. Temperature	-40°C ≤ T <sub>A</sub> ≤ +85°C		±0.18		dB
Attenuation Range	Between maximum and minimum attenuation states		30.8		dB
Attenuation Step Error	All attenuation states		±0.15		dB
Attenuation Absolute Error	All attenuation states		±0.35		dB
Input Return Loss			-10.3		dB
Output Return Loss			-9.6		dB
Input 1 dB Compression Point			31.5		dBm
Input Third-Order Intercept	Δf = 1 MHz, P <sub>OUT</sub> = 5 dBm/tone		44.7		dBm

Parameter	Conditions	Min	Typ	Max	Unit
DSA FREQUENCY = 2140 MHz	Using the DSAIN and DSAOUT pins, minimum attenuation				
Insertion Loss			-2.6		dB
vs. Frequency	±30 MHz		±0.02		dB
vs. Temperature	-40°C ≤ T <sub>A</sub> ≤ +85°C		±0.19		dB
Attenuation Range	Between maximum and minimum attenuation states		30.9		dB
Attenuation Step Error	All attenuation states		±0.13		dB
Attenuation Absolute Error	All attenuation states		±0.32		dB
Input Return Loss			-9.8		dB
Output Return Loss			-9.3		dB
Input 1 dB Compression Point			31.5		dBm
Input Third-Order Intercept	Δf = 1 MHz, P <sub>OUT</sub> = 5 dBm/tone		44.6		dBm
DSA FREQUENCY = 2630 MHz	Using the DSAIN and DSAOUT pins, minimum attenuation				
Insertion Loss			-2.8		dB
vs. Frequency	±60 MHz		±0.02		dB
vs. Temperature	-40°C ≤ T <sub>A</sub> ≤ +85°C		±0.21		dB
Attenuation Range	Between maximum and minimum attenuation states		31.2		dB
Attenuation Step Error	All attenuation states		±0.18		dB
Attenuation Absolute Error	All attenuation states		±0.24		dB
Input Return Loss			-10.0		dB
Output Return Loss			-9.6		dB
Input 1 dB Compression Point			31.5		dBm
Input Third-Order Intercept	Δf = 1 MHz, P <sub>OUT</sub> = 5 dBm/tone		43.8		dBm
DSA FREQUENCY = 3600 MHz	Using the DSAIN and DSAOUT pins, minimum attenuation				
Insertion Loss			-3.0		dB
vs. Frequency	±100 MHz		±0.02		dB
vs. Temperature	-40°C ≤ T <sub>A</sub> ≤ +85°C		±0.23		dB
Attenuation Range	Between maximum and minimum attenuation states		31.7		dB
Attenuation Step Error	All attenuation states		±0.38		dB
Attenuation Absolute Error	All attenuation states		±0.18		dB
Input Return Loss			-12.3		dB
Output Return Loss			-11.7		dB
Input 1 dB Compression Point			31.0		dBm
Input Third-Order Intercept	Δf = 1 MHz, P <sub>OUT</sub> = 5 dBm/tone		42.2		dBm
DSA Gain Settling	Using the DSAIN and DSAOUT pins				
Minimum Attenuation to Maximum Attenuation			36		ns
Maximum Attenuation to Minimum Attenuation			36		ns
LOOP FREQUENCY = 943 MHz	AMP1-DSA-AMP2, DSA at minimum attenuation				
Gain			34.0		dB
vs. Frequency	±18 MHz		±0.10		dB
Gain Range	Between maximum and minimum attenuation states		29.3		dB
Input Return Loss	S11		-14.2		dB
Output Return Loss	S22		-10.1		dB
Output 1 dB Compression Point			25.1		dBm
Output Third-Order Intercept	Δf = 1 MHz, P <sub>OUT</sub> = 5 dBm/tone		42.8		dBm
Noise Figure			2.9		dB

Parameter	Conditions	Min	Typ	Max	Unit
LOOP FREQUENCY = 2140 MHz	AMP1 – DSA – AMP2, DSA at minimum attenuation				
Gain			31.3		dB
vs. Frequency	±30 MHz		±0.03		dB
Gain Range	Between maximum and minimum attenuation states		32.5		dB
Input Return Loss	S11		-9.3		dB
Output Return Loss	S22		-5.4		dB
Output 1 dB Compression Point			25.3		dBm
Output Third-Order Intercept	Δf = 1 MHz, P <sub>OUT</sub> = 5 dBm/tone		40.0		dBm
Noise Figure			3.1		dB
LOOP FREQUENCY = 2630 MHz	AMP1 – DSA – AMP2, DSA at minimum attenuation				
Gain			29.5		dB
vs. Frequency	±60 MHz		±0.56		dB
Gain Range	Between maximum and minimum attenuation states		30.0		dB
Input Return Loss	S11		-12.6		dB
Output Return Loss	S22		-5.8		dB
Output 1 dB Compression Point			24.6		dBm
Output Third-Order Intercept	Δf = 1 MHz, P <sub>OUT</sub> = 5 dBm/tone		39.3		dBm
Noise Figure			3.1		dB
POWER SUPPLIES					
Voltage		4.75	5.0	5.25	V
Supply Current	AMP1		89	120	mA
	AMP2		86	120	mA
	DSA		0.5		mA



## ABSOLUTE MAXIMUM RATINGS

Table 2.

Parameter	Rating
Supply Voltage (VDD, VCC, VCC2)	6.5 V
Input Power	
AMP1IN	16 dBm
AMP2IN (50 $\Omega$ Impedance)	20 dBm
DSAIN	30 dBm
Internal Power Dissipation	1.0 W
$\theta_{JA}$ (Exposed Paddle Soldered Down)	34.8°C/W
$\theta_{JC}$ (Exposed Paddle)	6.2°C/W
Maximum Junction Temperature	150°C
Lead Temperature (Soldering, 60 sec)	240°C
Operating Temperature Range	-40°C to +85°C
Storage Temperature Range	-65°C to +150°C

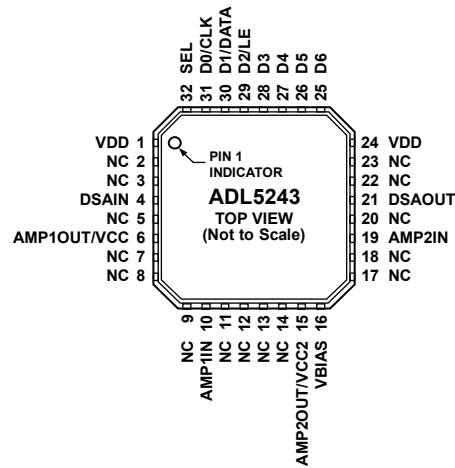
Stresses above those listed under Absolute Maximum Ratings may cause permanent damage to the device. This is a stress rating only; functional operation of the device at these or any other conditions above those indicated in the operational section of this specification is not implied. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

### ESD CAUTION



**ESD (electrostatic discharge) sensitive device.** Charged devices and circuit boards can discharge without detection. Although this product features patented or proprietary protection circuitry, damage may occur on devices subjected to high energy ESD. Therefore, proper ESD precautions should be taken to avoid performance degradation or loss of functionality.

## PIN CONFIGURATION AND FUNCTION DESCRIPTIONS



- NOTES  
 1. NC = NO CONNECT. DO NOT CONNECT TO THIS PIN.  
 2. THE EXPOSED PAD MUST BE CONNECTED TO GROUND.

09431-002

Figure 2. Pin Configuration

Table 3. Pin Function Descriptions

Pin No.	Mnemonic	Description
1, 24	VDD	Supply Voltage for DSA. Connect this pin to a 5 V supply.
2, 3, 5, 7, 8, 9, 11, 12, 13, 14, 17, 18, 20, 22, 23	NC	No Connect. Do not connect to this pin.
4	DSAIN	RF Input to DSA.
6	AMP1OUT/VCC	RF Output from Amplifier 1/Supply Voltage for Amplifier 1. Bias to Gain Block Amplifier 1 is provided through a choke to this pin when connected to VCC.
10	AMP1IN	RF Input to Gain Block Amplifier 1.
15	AMP2OUT/VCC2	RF Output from Amplifier 2/Supply Voltage for Amplifier 2. Bias to Driver Amplifier 2 is provided through a choke to this pin when connected to VCC2.
16	VBIAS	Bias for Driver Amplifier 2.
19	AMP2IN	RF Input to Amplifier 2.
21	DSAOUT	RF Output from DSA.
25	D6	Data Bit in Parallel Mode (LSB). Connect to supply in serial mode.
26	D5	Data Bit in Parallel Mode. Connect to ground in serial mode.
27	D4	Data Bit in Parallel Mode. Connect to ground in serial mode.
28	D3	Data Bit in Parallel Mode. Connect to ground in serial mode.
29	D2/LE	Data Bit in Parallel Mode/Latch Enable in Serial Mode.
30	D1/DATA	Data Bit in Parallel Mode (MSB)/Data in Serial Mode.
31	D0/CLK	Connect this pin to ground in parallel mode. This pin functions as a clock in serial mode.
32	SEL	Select Pin. Connect this pin to the supply for parallel mode operation; connect this pin to ground for serial mode operation.
	EPAD	Exposed Paddle. The exposed paddle must be connected to ground.

# TYPICAL PERFORMANCE CHARACTERISTICS

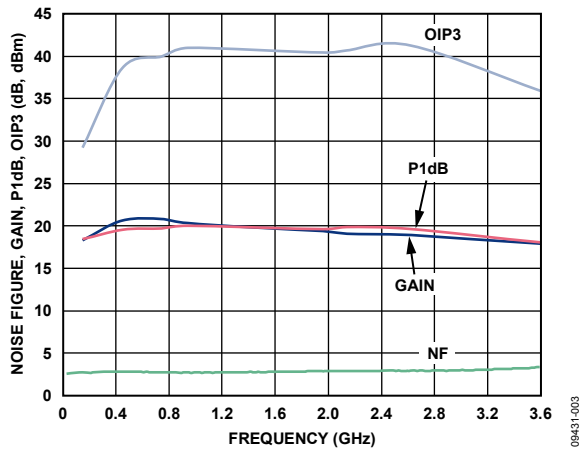


Figure 3. AMP1: Gain, P1dB, OIP3 at  $P_{OUT} = 3$  dBm/Tone and Noise Figure vs. Frequency

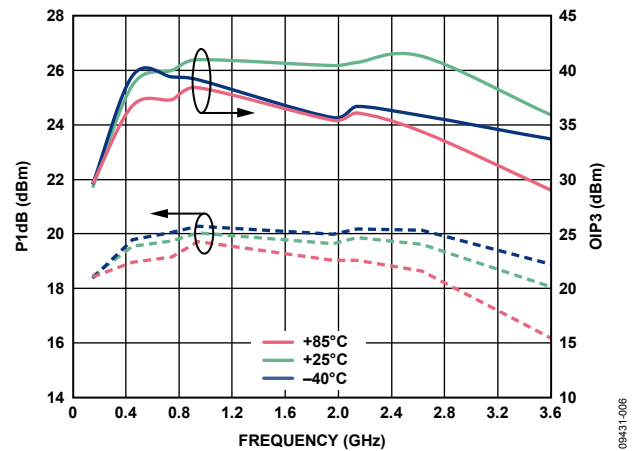


Figure 6. AMP1: OIP3 at  $P_{out} = 3$  dBm/Tone and P1dB vs. Frequency and Temperature

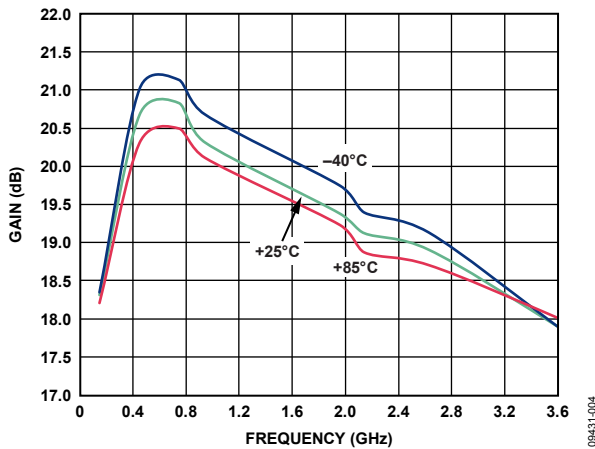


Figure 4. AMP1: Gain vs. Frequency and Temperature

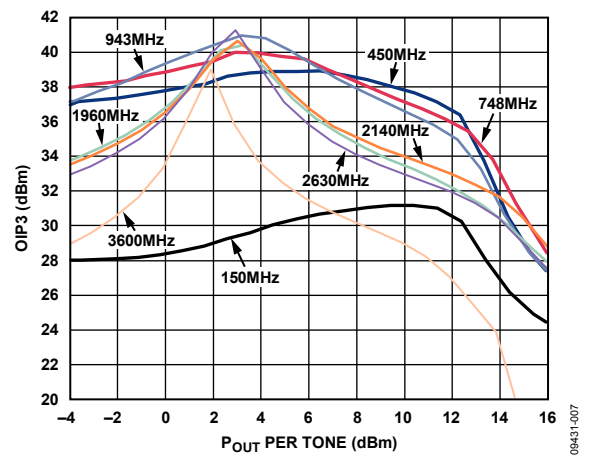


Figure 7. AMP1: OIP3 vs.  $P_{OUT}$  and Frequency

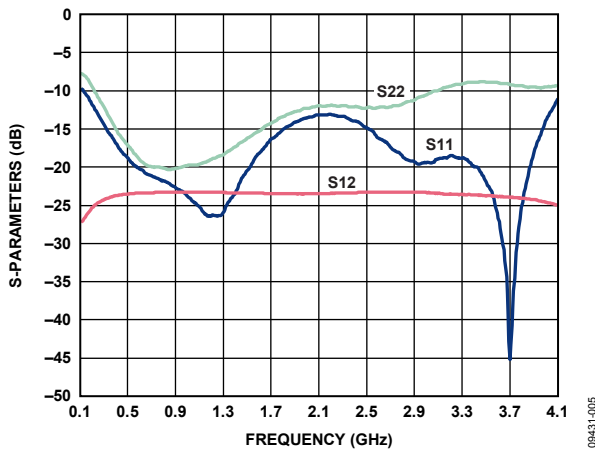


Figure 5. AMP1: Input Return Loss (S11), Output Return Loss (S22), and Reverse Isolation (S12) vs. Frequency

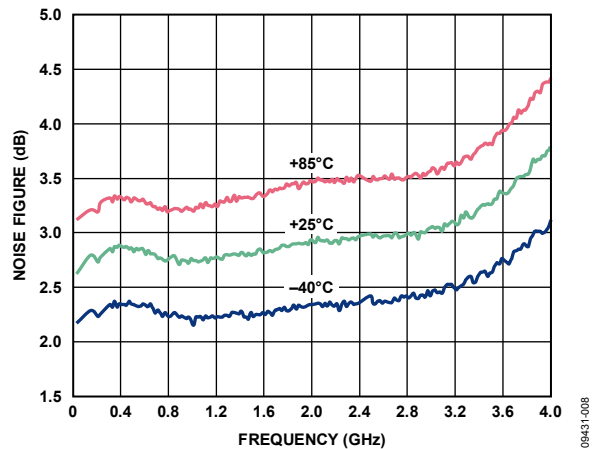


Figure 8. AMP1: Noise Figure vs. Frequency and Temperature

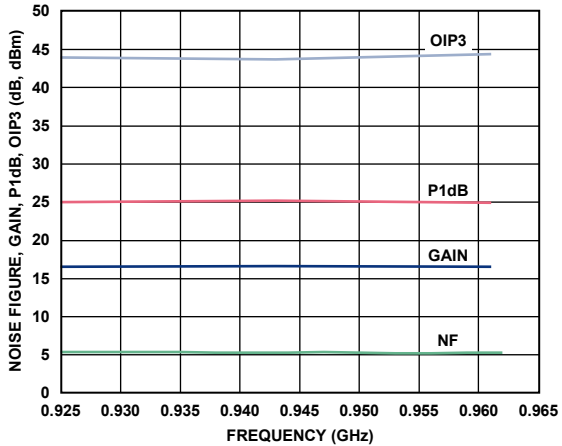


Figure 9. AMP2-943 MHz: Gain, P1dB, OIP3 at  $P_{OUT} = 5$  dBm/Tone and Noise Figure vs. Frequency

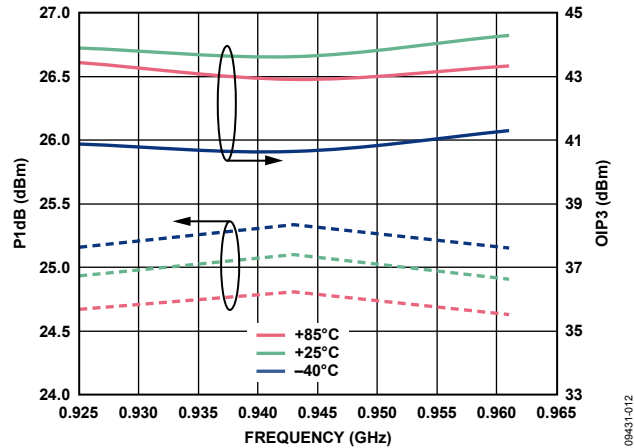


Figure 12. AMP2-943 MHz: OIP3 at  $P_{OUT} = 5$  dBm/Tone and P1dB vs. Frequency and Temperature

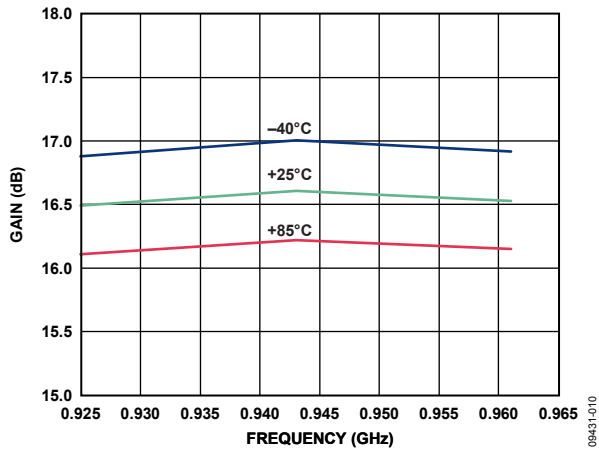


Figure 10. AMP2-943 MHz: Gain vs. Frequency and Temperature

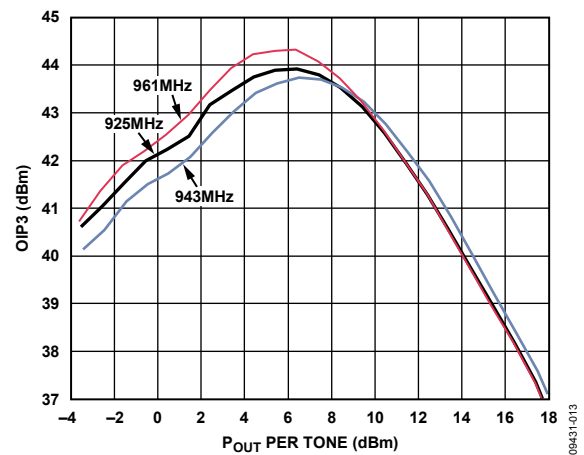


Figure 13. AMP2-943 MHz: OIP3 vs.  $P_{OUT}$  and Frequency

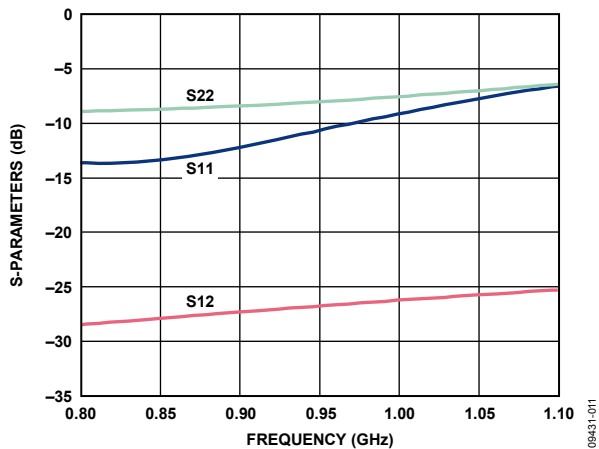


Figure 11. AMP2-943 MHz: Input Return Loss (S11), Output Return Loss (S22) and Reverse Isolation (S12) vs. Frequency

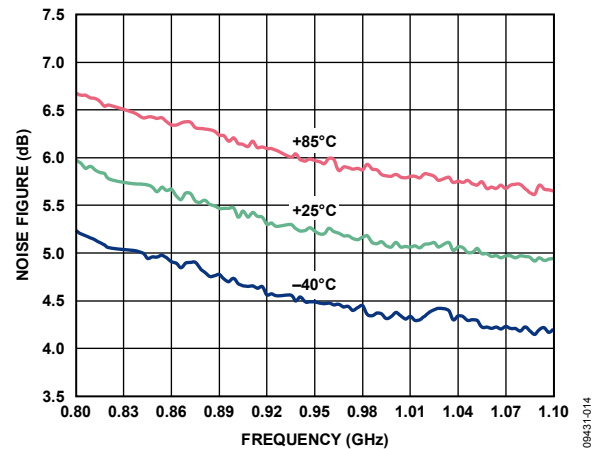


Figure 14. AMP2-943 MHz: Noise Figure vs. Frequency and Temperature

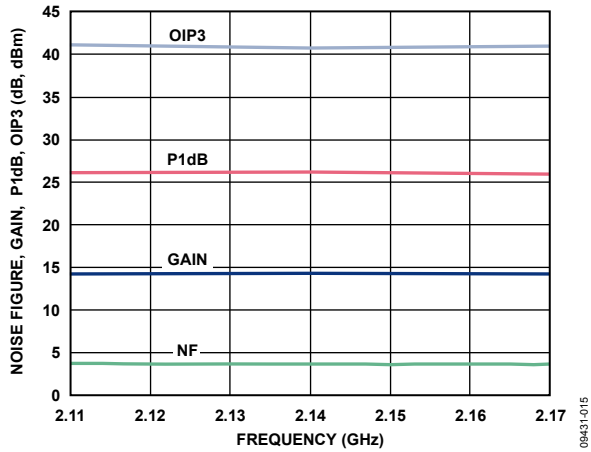


Figure 15. AMP2-2140 MHz: Gain, P1dB, OIP3 at  $P_{OUT} = 5$  dBm/Tone and Noise Figure vs. Frequency

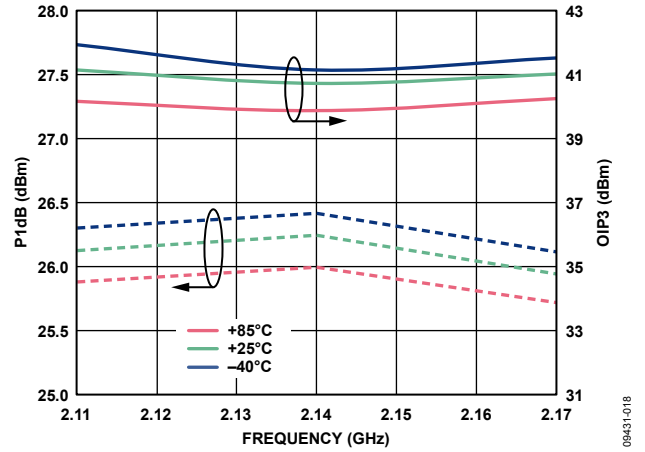


Figure 18. AMP2-2140 MHz: OIP3 at  $P_{OUT} = 5$  dBm/Tone and P1dB vs. Frequency and Temperature

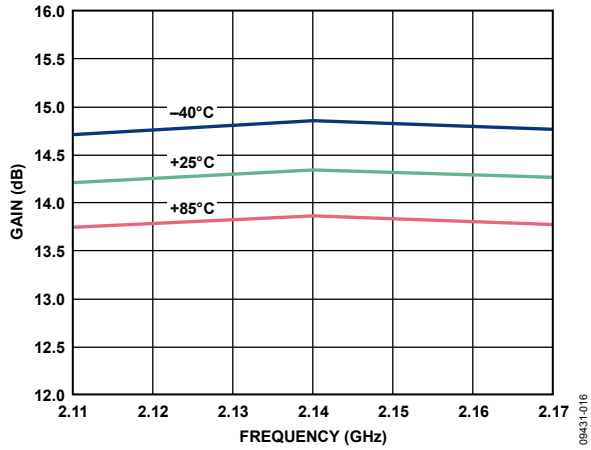


Figure 16. AMP2-2140 MHz: Gain vs. Frequency and Temperature

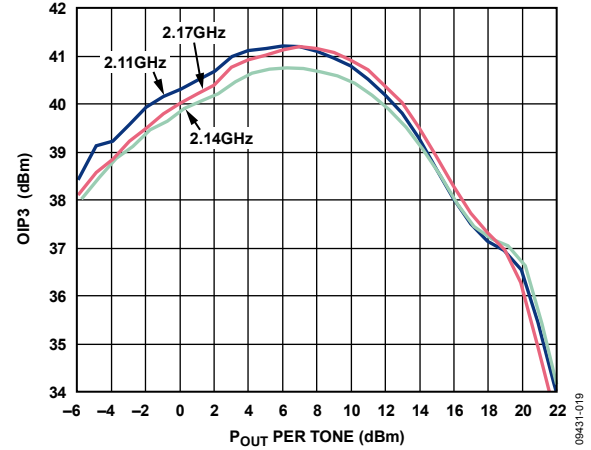


Figure 19. AMP2-2140 MHz: OIP3 vs.  $P_{OUT}$  and Frequency

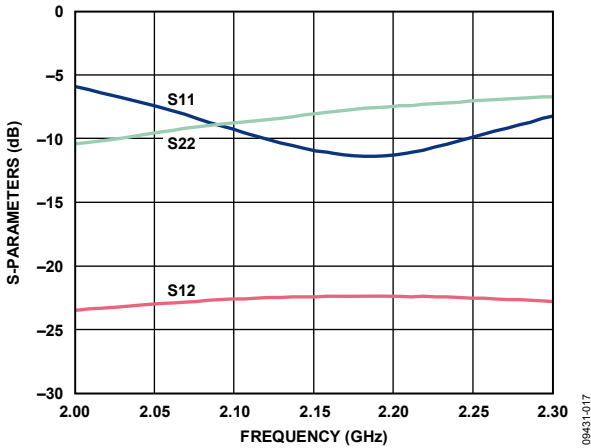


Figure 17. AMP2-2140 MHz: Input Return Loss (S11), Output Return Loss (S22), and Reverse Isolation (S12) vs. Frequency

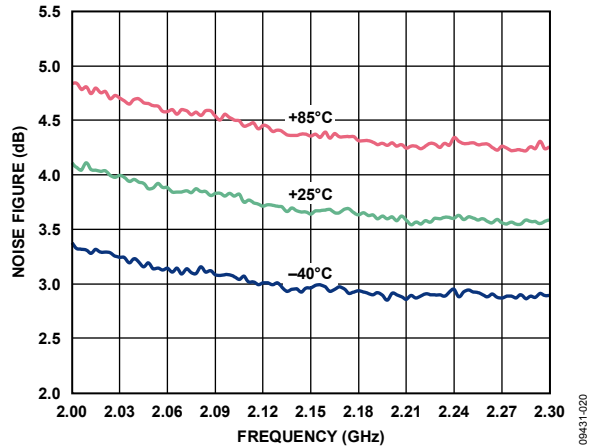


Figure 20. AMP2-2140 MHz: Noise Figure vs. Frequency and Temperature

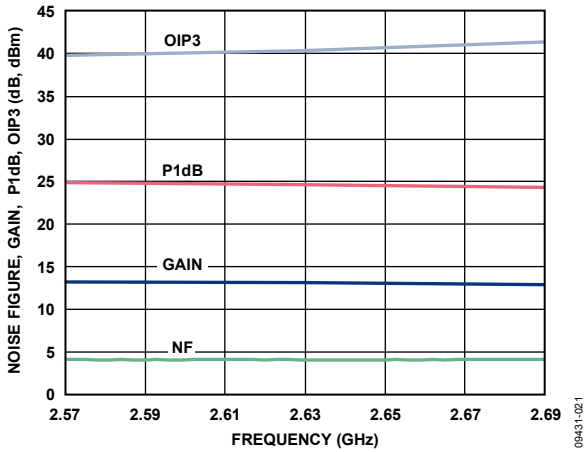


Figure 21. AMP2-2630 MHz: Gain, P1dB, OIP3 at  $P_{OUT} = 5$  dBm/Tone and Noise Figure vs. Frequency

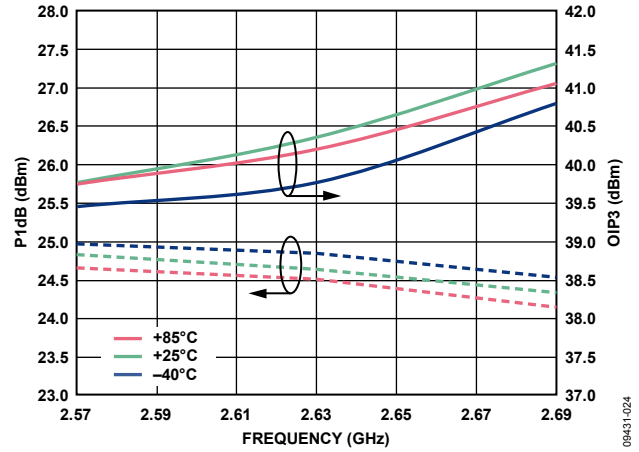


Figure 24. AMP2-2630 MHz: OIP3 at  $P_{OUT} = 5$  dBm/Tone and P1dB vs. Frequency and Temperature

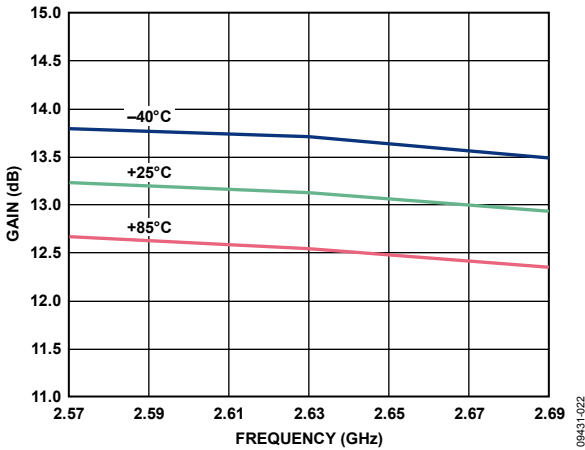


Figure 22. AMP2-2630 MHz: Gain vs. Frequency and Temperature

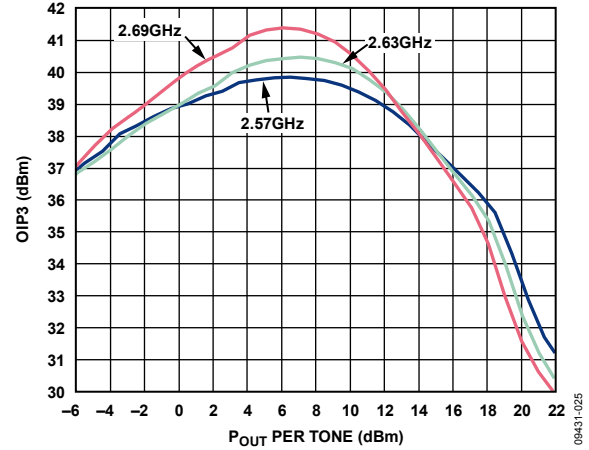


Figure 25. AMP2-2630 MHz: OIP3 vs.  $P_{OUT}$  and Frequency

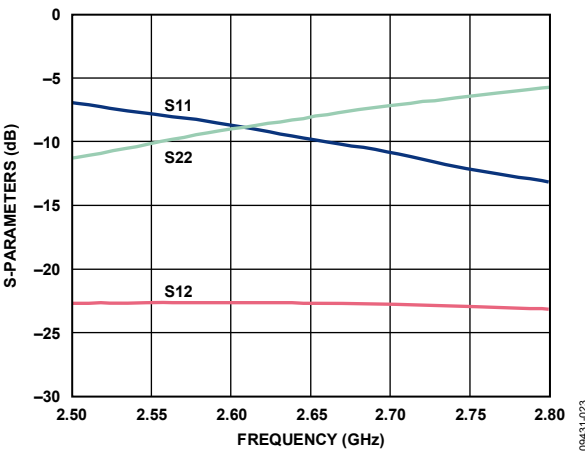


Figure 23. AMP2-2630 MHz: Input Return Loss (S11), Output Return Loss (S22), and Reverse Isolation (S12) vs. Frequency

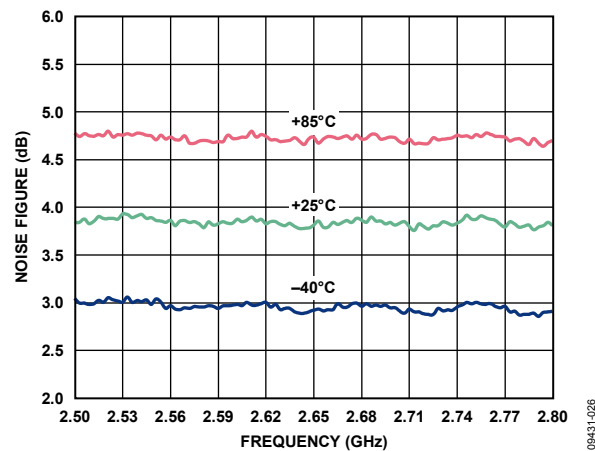


Figure 26. AMP2-2630 MHz: Noise Figure vs. Frequency and Temperature

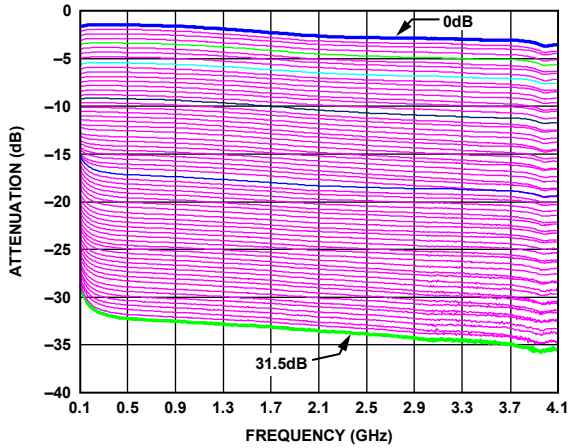


Figure 27. DSA: Attenuation vs. Frequency

09431-027

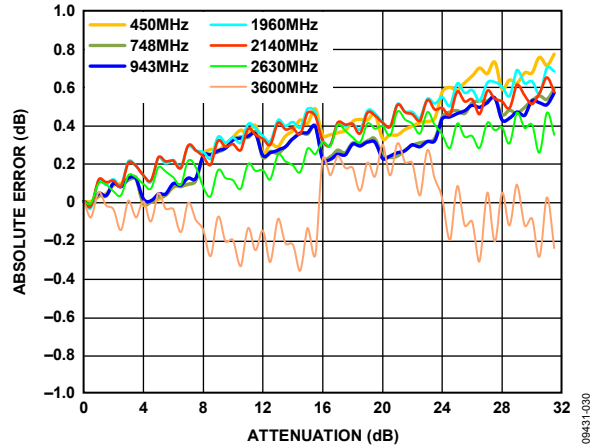


Figure 30. DSA: Absolute Error vs. Attenuation

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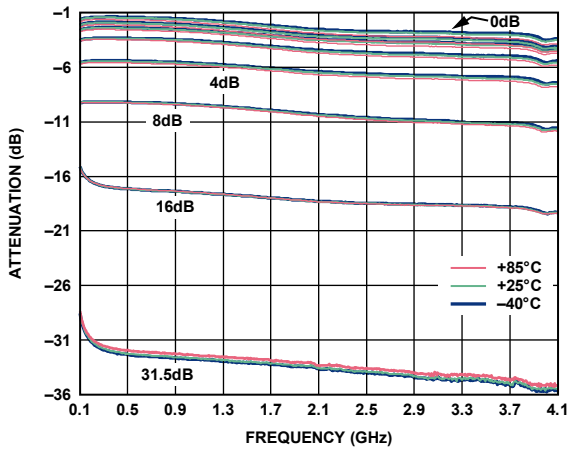


Figure 28. DSA: Attenuation vs. Frequency and Temperature

09431-028

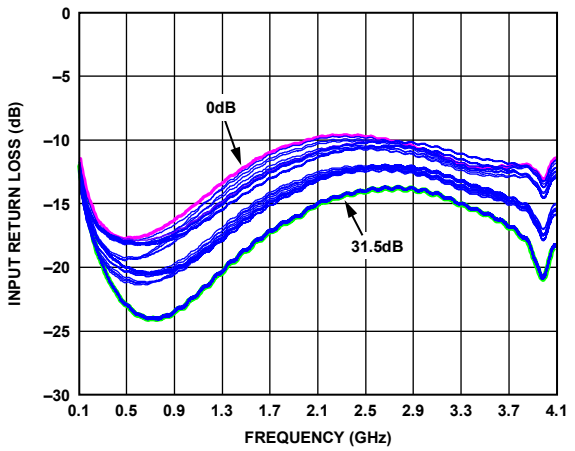


Figure 31. DSA: Input Return Loss vs. Frequency, All States

09431-031

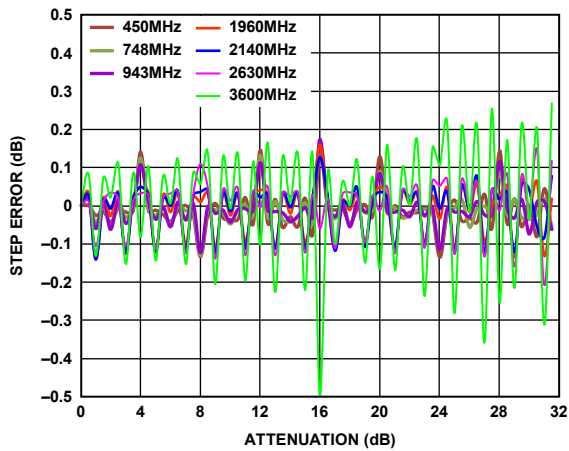


Figure 29. DSA: Step Error vs. Attenuation

09431-029

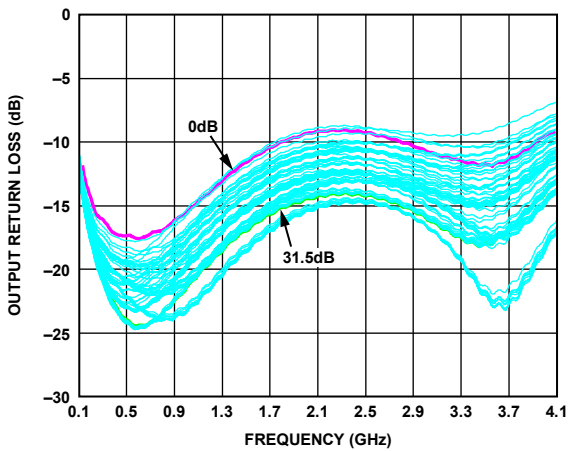


Figure 32. DSA: Output Return Loss vs. Frequency, All States

09431-032

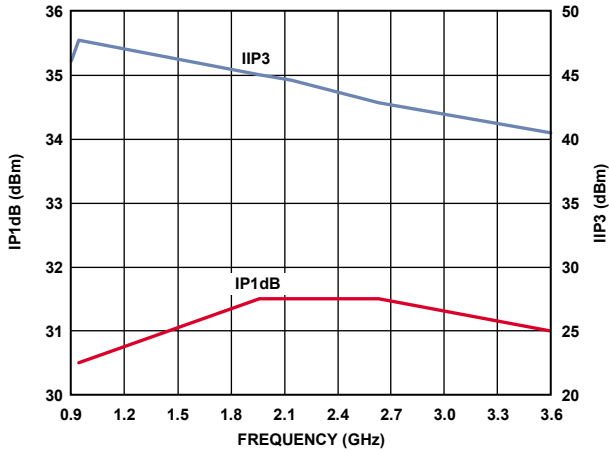


Figure 33. DSA: Input P1dB and Input IP3 vs. Frequency, Minimum Attenuation State

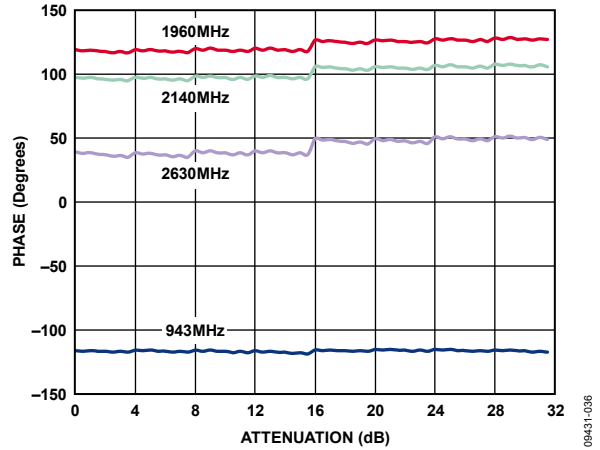


Figure 36. DSA: Phase vs. Attenuation

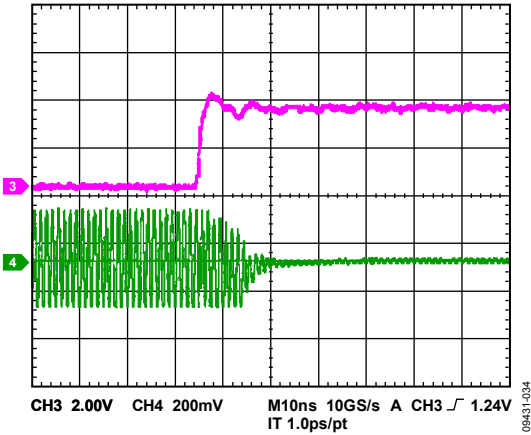


Figure 34. DSA: Gain Settling Time, 0 dB to 31.5 dB

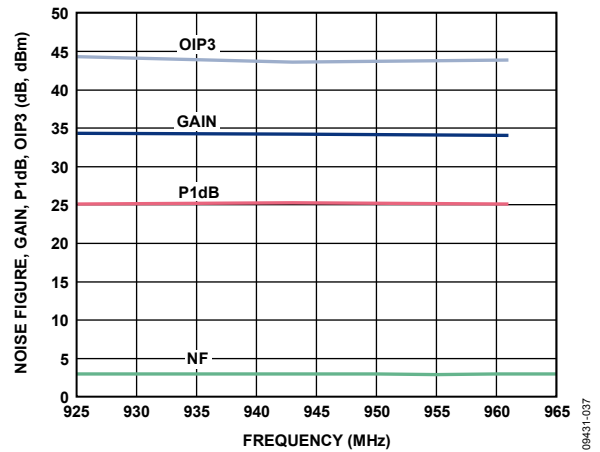


Figure 37. Loop-943 MHz: Gain, P1dB, OIP3 at  $P_{OUT} = 5$  dBm/Tone and Noise Figure vs. Frequency, Minimum Attenuation State

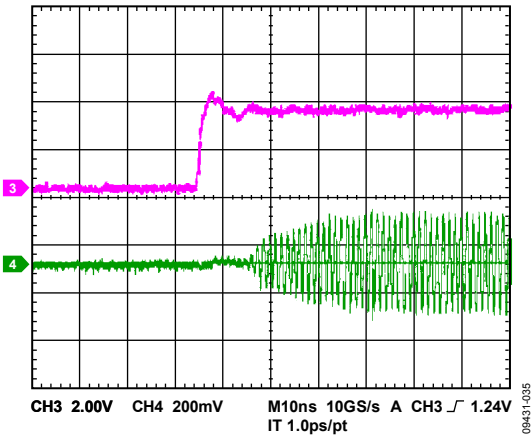


Figure 35. DSA: Gain Settling Time, 31.5 dB to 0 dB

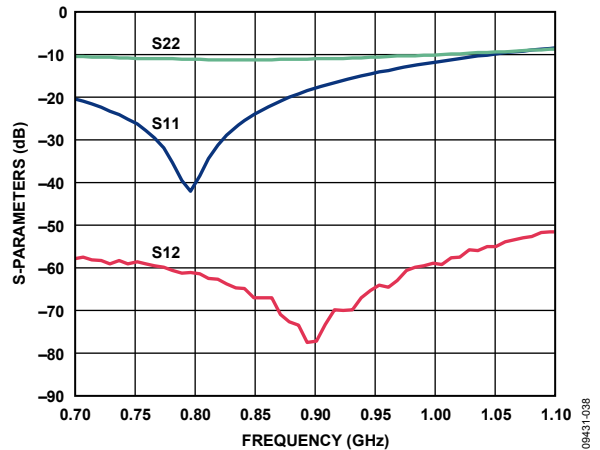


Figure 38. Loop-943 MHz: Input Return Loss (S11), Output Return Loss (S22), and Reverse Isolation (S12) vs. Frequency, Minimum Attenuation State



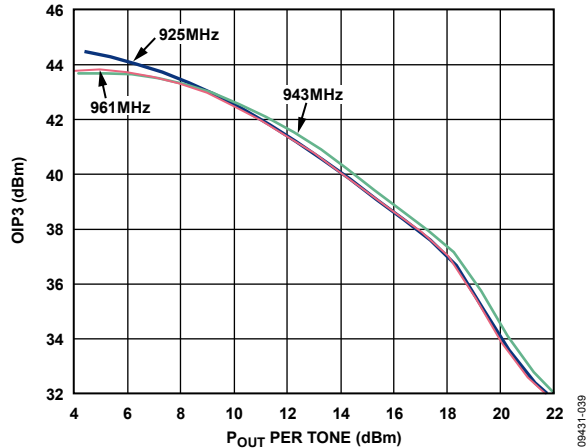


Figure 39. Loop-943 MHz: OIP3 vs.  $P_{OUT}$  and Frequency, Minimum Attenuation State

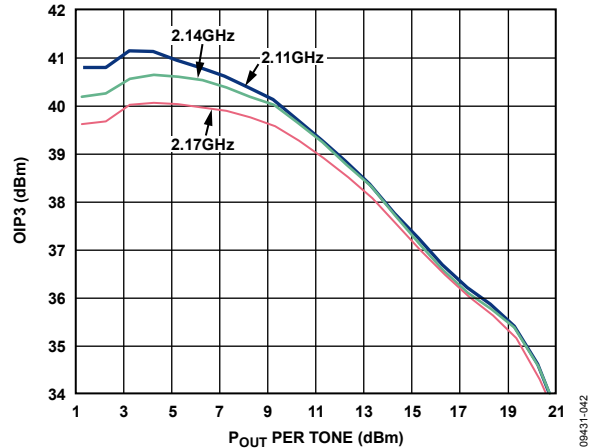


Figure 42. Loop-2140 MHz: OIP3 vs.  $P_{OUT}$  and Frequency, Minimum Attenuation State

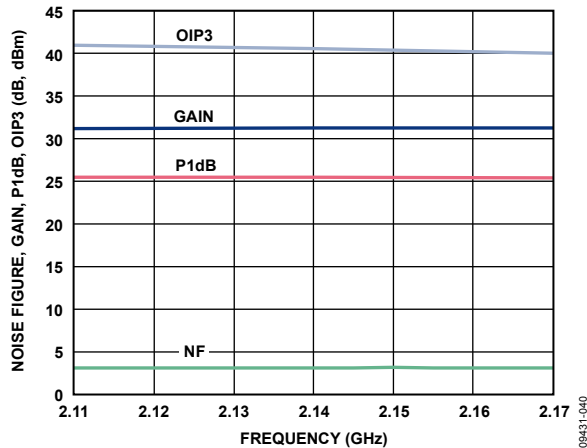


Figure 40. Loop-2140 MHz: Gain, P1dB, OIP3 at  $P_{OUT} = 5$  dBm/Tone and Noise Figure vs. Frequency, Minimum Attenuation State

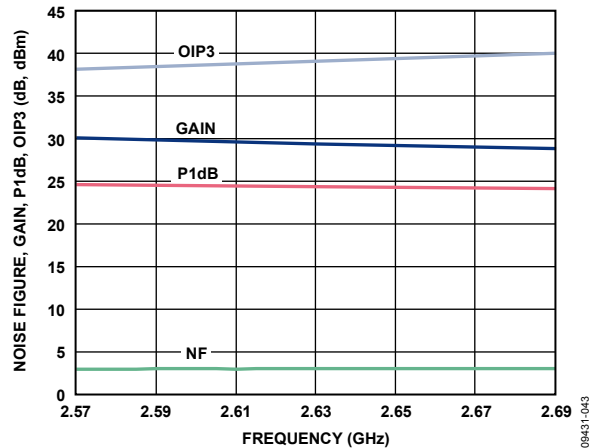


Figure 43. Loop-2630 MHz: Gain, P1dB, OIP3 at  $P_{OUT} = 5$  dBm/Tone and Noise Figure vs. Frequency, Minimum Attenuation State

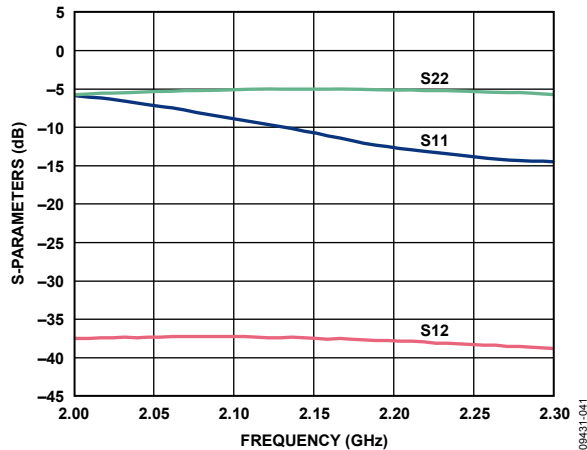


Figure 41. Loop-2140 MHz: Input Return Loss (S11), Output Return Loss

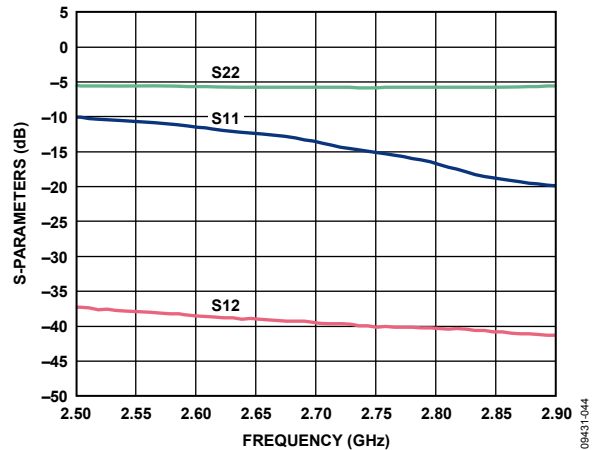


Figure 44. Loop-2630 MHz: Input Return Loss (S11), Output Return Loss (S22), and Reverse Isolation (S12) vs. Frequency, Minimum Attenuation State

(S22), and Reverse Isolation (S12) vs. Frequency, Minimum Attenuation State

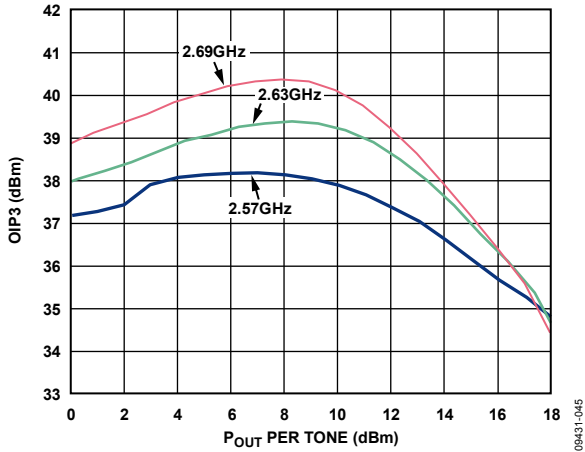


Figure 45. Loop-2630 MHz: OIP3 vs.  $P_{OUT}$  and Frequency, Minimum Attenuation State

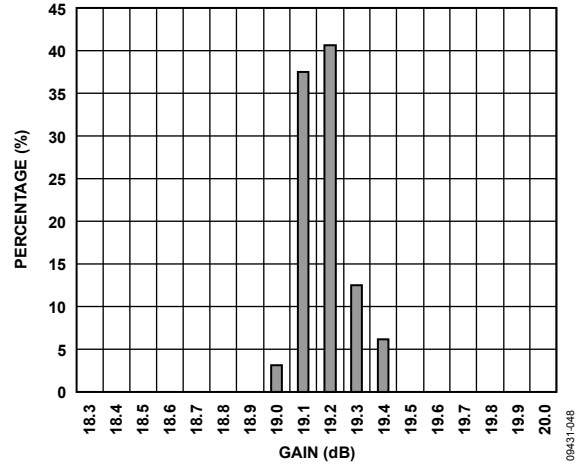


Figure 48. AMP1: Gain Distribution at 2140 MHz

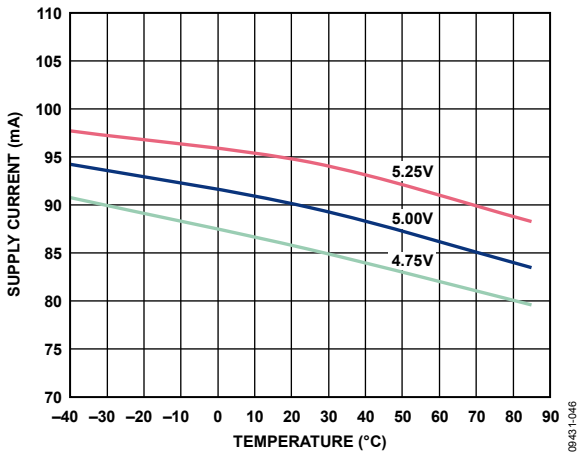


Figure 46. AMP1: Supply Current vs. Voltage and Temperature

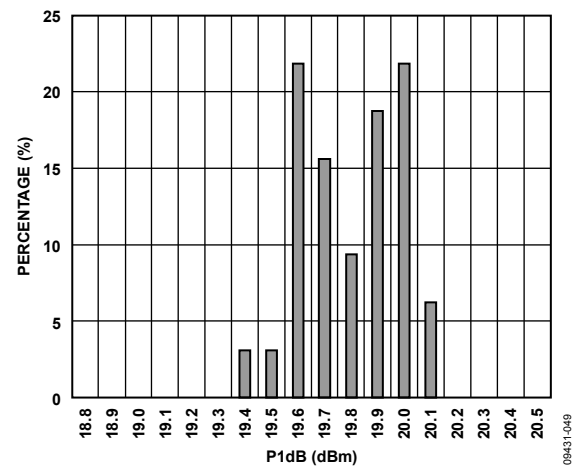


Figure 49. AMP1: P1dB Distribution at 2140 MHz

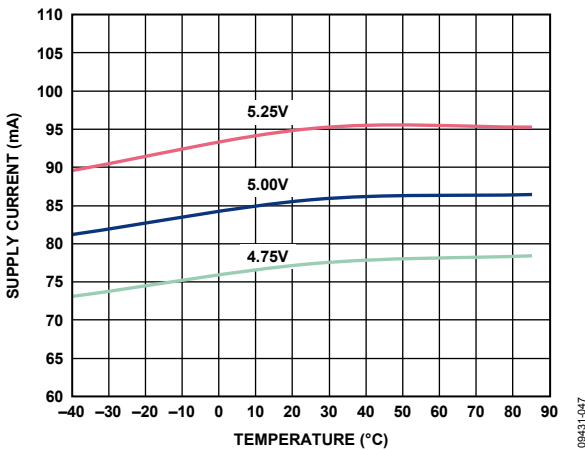


Figure 47. AMP2: Supply Current vs. Voltage and Temperature

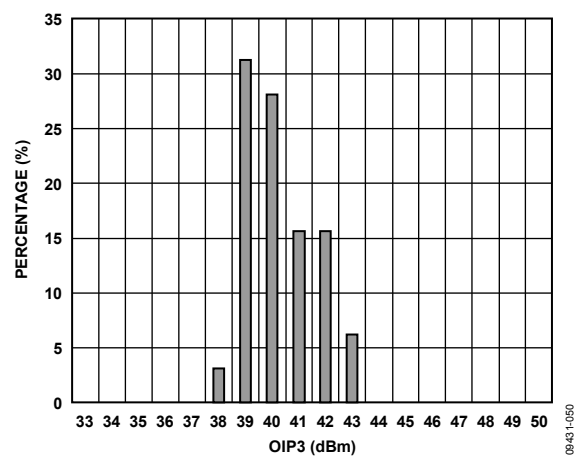


Figure 50. AMP1: OIP3 Distribution at 2140 MHz

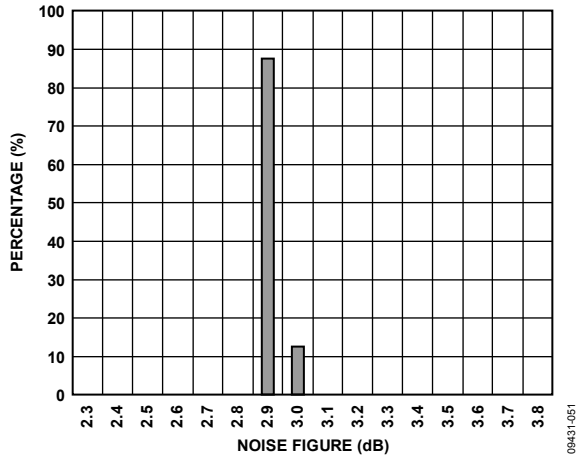


Figure 51. AMP1: Noise Figure Distribution at 2140 MHz

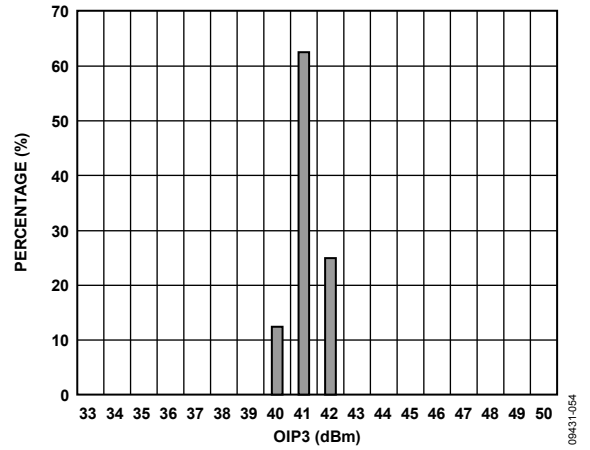


Figure 54. AMP2: OIP3 Distribution at 2140 MHz

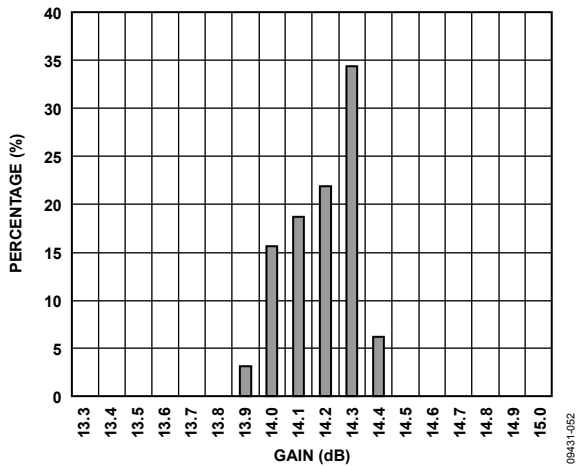


Figure 52. AMP2: Gain Distribution at 2140 MHz

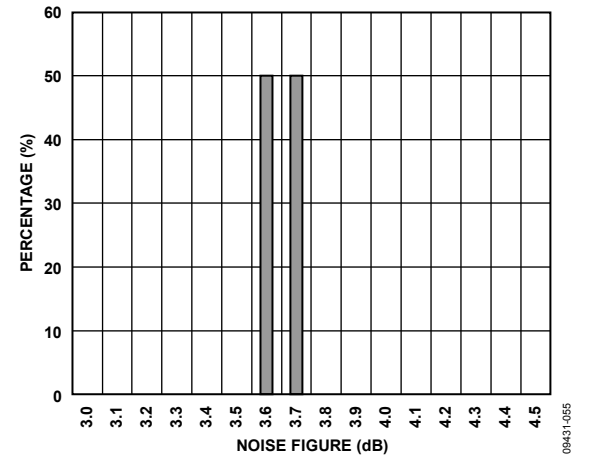


Figure 55. AMP2: Noise Figure Distribution at 2140 MHz

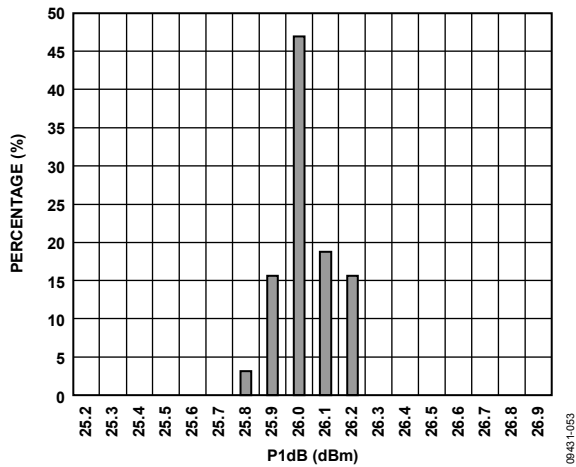


Figure 53. AMP2: P1dB Distribution at 2140 MHz

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# APPLICATIONS INFORMATION

## BASIC LAYOUT CONNECTIONS

The basic connections for operating the ADL5243 are shown in Figure 56. The schematic is configured for 2140 MHz operation.

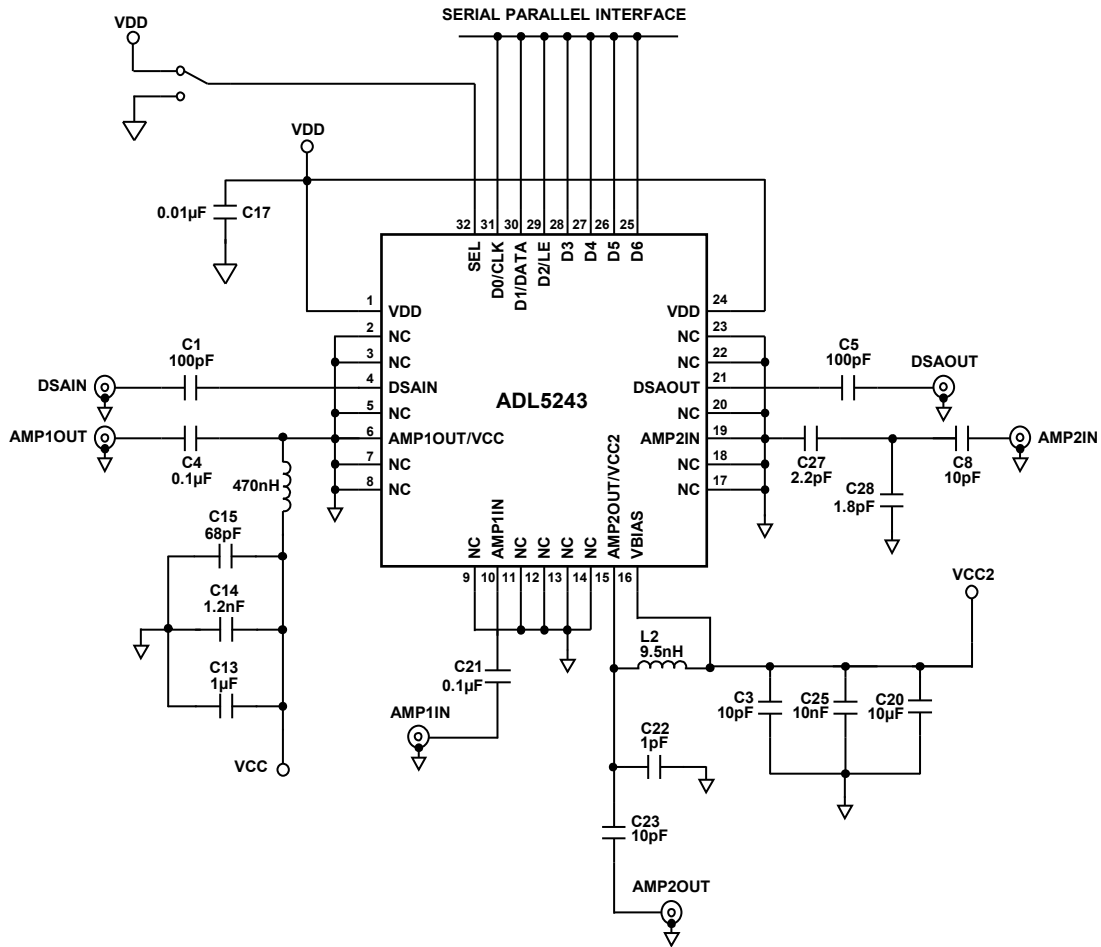


Figure 56. Basic Connections

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**Amplifier 1 Power Supply**

AMP1 in the ADL5243 is a broadband gain block. The dc bias is supplied through Inductor L1 and is connected to the AMP1OUT pin. Three decoupling capacitors (C13, C14, and C25) are used to prevent RF signals from propagating on the dc lines. The dc supply ranges from 4.75 V to 5.25 V and should be connected to the VCC test pin.

**Amplifier 1 RF Input Interface**

Pin 10 is the RF input for AMP1 of the ADL5243. The amplifier is internally matched to 50  $\Omega$  at the input; therefore, no external components are required. Only a dc blocking capacitor (C21) is required.

**Amplifier 1 RF Output Interface**

Pin 6 is the RF output for AMP1 of the ADL5243. The amplifier is internally matched to 50  $\Omega$  at the output as well; therefore, no external components are required. Only a dc blocking capacitor (C4) is required. The bias is provided through this pin via a choke inductor, L1.

**Amplifier 2 Power Supply**

The collector bias for AMP2 is supplied through Inductor L2 and is connected to the AMP2OUT pin, whereas the base bias is provided through Pin 16. The base bias is connected to the same supply pin as the collector bias. Three decoupling capacitors (C3, C20, and C25) are used to prevent RF signals from propagating on the dc lines. The dc supply ranges from 4.75 V to 5.25 V and should be connected to the VCC2 test pin.

**Amplifier 2 RF Input Interface**

Pin 19 is the RF input for AMP2 of the ADL5243. The input of the amplifier is easily matched to 50  $\Omega$  with a combination of series and shunt capacitors and a microstrip line serving as an inductor. Figure 56 shows the input matching components and is configured for 2140 MHz.

**Amplifier 2 RF Output Interface**

Pin 15 is the RF input for AMP2 of the ADL5243. The output of the amplifier is easily matched to 50  $\Omega$  with a combination of series and shunt capacitors and a microstrip line serving as an inductor.

Additionally, bias is provided through this pin. Figure 56 shows the output matching components and is configured for 2140 MHz.

**DSA RF Input Interface**

Pin 4 is the RF input for the DSA of the ADL5243. The input impedance of the DSA is close to 50  $\Omega$  over the entire frequency range; therefore, no external components are required. Only a dc blocking capacitor (C1) is required.

**DSA RF Output Interface**

Pin 21 is the RF output for the DSA of the ADL5243. The output impedance of the DSA is close to 50  $\Omega$  over the entire frequency range; therefore, no external components are required. Only a dc blocking capacitor (C5) is required.

**DSA SPI Interface**

The DSA of the ADL5243 can operate in either serial or parallel mode. Pin 32 (SEL) controls the mode of operation. For serial mode operation, connect SEL to ground, and for parallel mode operation, connect SEL to VDD. In parallel mode, Pin 25 to Pin 30 (D6 to D1) are the data bits, with D6 being the LSB. Connect Pin 31 (D0) to ground during parallel mode of operation. In serial mode, Pin 29 is the latch enable (LE), Pin 30 is the data (DATA), and Pin 31 is the clock (CLK). Pin 26, Pin 27, and Pin 28 are not used in the serial mode and should be connected to ground. Pin 25 (D6) should be connected to VDD during the serial mode of operation. To prevent noise from coupling onto the digital signals, an RC filter can be used on each data line.

**SPI TIMING****SPI Timing Sequence**

Figure 58 shows the timing sequence for the SPI function using a 6-bit operation. The clock can be as fast as 20 MHz. In serial mode operation, Register B5 (MSB) is first, and Register B0 (LSB) is last.

**Table 4. Mode Selection Table**

Pin 32 (SEL)	Functionality
Connect to Ground	Serial mode
Connect to Supply	Parallel mode

**Table 5. SPI Timing Specifications**

Parameter	Limit	Unit	Test Conditions/Comments
F <sub>CLK</sub>	10	MHz	Data clock frequency
t <sub>1</sub>	30	ns min	Clock high time
t <sub>2</sub>	30	ns min	Clock low time
t <sub>3</sub>	10	ns min	Data to clock setup time
t <sub>4</sub>	10	ns min	Clock to data hold time
t <sub>5</sub>	10	ns min	Clock low to LE setup time
t <sub>6</sub>	30	ns min	LE pulse width

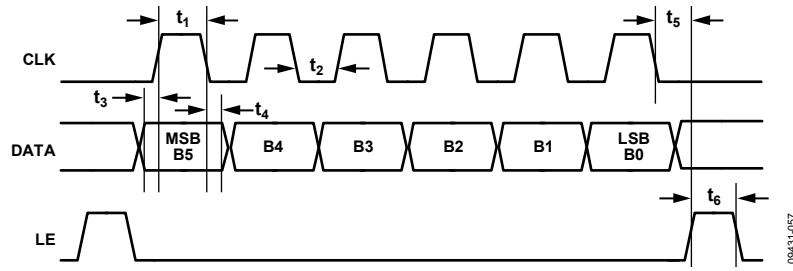


Figure 57. SPI Timing Diagram (Data Loaded MSB First)

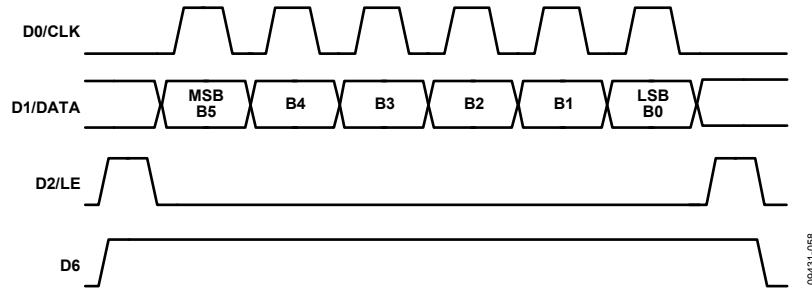


Figure 58. SPI Timing Sequence

Table 6. DSA Attenuation Truth Table—Serial Mode

Attenuation State	B5 (MSB)	B4	B3	B2	B1	B0 (LSB)
0 dB (Reference)	1	1	1	1	1	1
0.5 dB	1	1	1	1	1	0
1.0 dB	1	1	1	1	0	1
2.0 dB	1	1	1	0	1	1
4.0 dB	1	1	0	1	1	1
8.0 dB	1	0	1	1	1	1
16.0 dB	0	1	1	1	1	1
31.5 dB	0	0	0	0	0	0

Table 7. DSA Attenuation Truth Table—Parallel Mode

Attenuation State	D1 (MSB)	D2	D3	D4	D5	D6 (LSB)
0 dB (Reference)	1	1	1	1	1	1
0.5 dB	1	1	1	1	1	0
1.0 dB	1	1	1	1	0	1
2.0 dB	1	1	1	0	1	1
4.0 dB	1	1	0	1	1	1
8.0 dB	1	0	1	1	1	1
16.0 dB	0	1	1	1	1	1
31.5 dB	0	0	0	0	0	0

**ADL5243 AMPLIFIER 2 MATCHING**

The AMP2 input and output of the ADL5243 can be easily matched to 50  $\Omega$  with two or three external components and the microstrip line used as an inductor. Table 8 lists the required matching components values. All capacitors are Murata GRM155 series (0402 size), and Inductor L1 is a Coilcraft® 0603CS series (0603 size). For all frequency bands, the

placement of Capacitors C22, C26, and C28 is critical. Table 9 lists the recommended component spacing of C22, C26, and C28 for the various frequencies. The component spacing is referenced from the center of the component to the edge of the package. Figure 59 to Figure 62 show the graphical representation of the matching network.

**Table 8. Component Values**

Frequency	C27	C26	C28	C8	C22	C23	L2	R10	R12
748 MHz	0 $\Omega$	Open	5.1 pF	12 pF	1.3 pF	100 pF	56 nH	18 $\Omega$	3.9 nH
943 MHz	0 $\Omega$	3.9 pF	Open	6 pF	1.3 pF	100 pF	56 nH	18 $\Omega$	3.3 nH
2140 MHz	2.2 pF	Open	1.8 pF	10 pF	1 pF	10 pF	9.5 nH	0 $\Omega$	0 $\Omega$
2630 MHz	2.7 pF	1.1 pF	Open	10 pF	1.3 pF	20 pF	9.5 nH	0 $\Omega$	0 $\Omega$

**Table 9. Component Spacing**

Frequency	C26: $\lambda 1$ (mils)	C28: $\lambda 2$ (mils)	C22: $\lambda 3$ (mils)
748 MHz	N/A	315	201
943 MHz	236	N/A	394
2140 MHz	N/A	366	244
2630 MHz	126	N/A	240

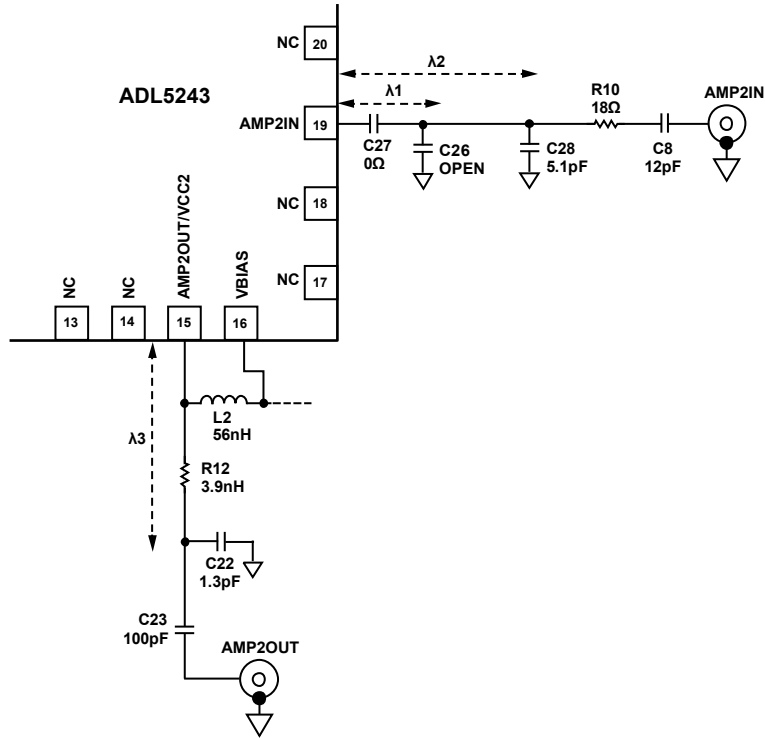


Figure 59. AMP2: Matching Circuit at 748 MHz

09431-061

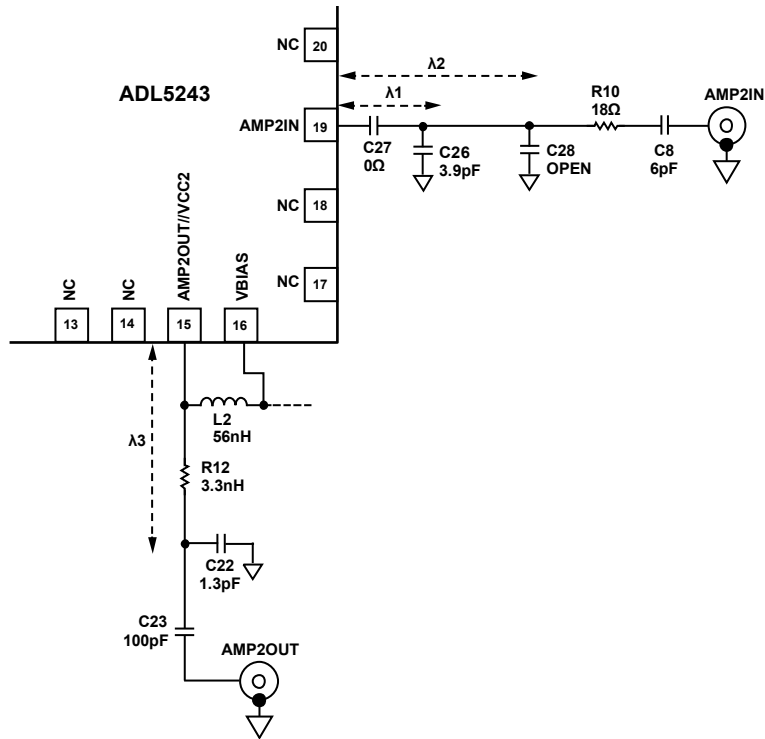


Figure 60. AMP2: Matching Circuit at 943 MHz

09431-062



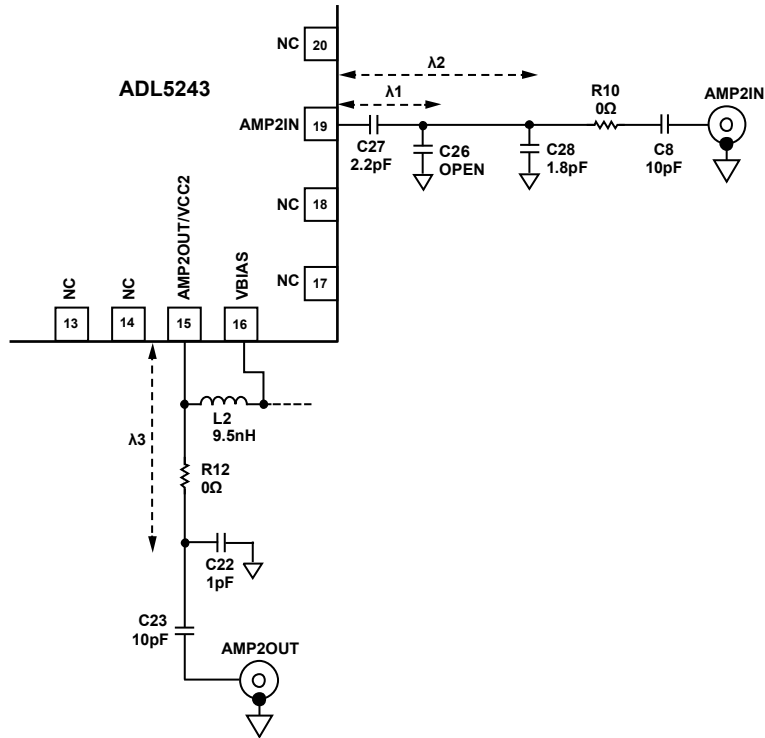


Figure 61. AMP2: Matching Circuit at 2140 MHz

09431-064

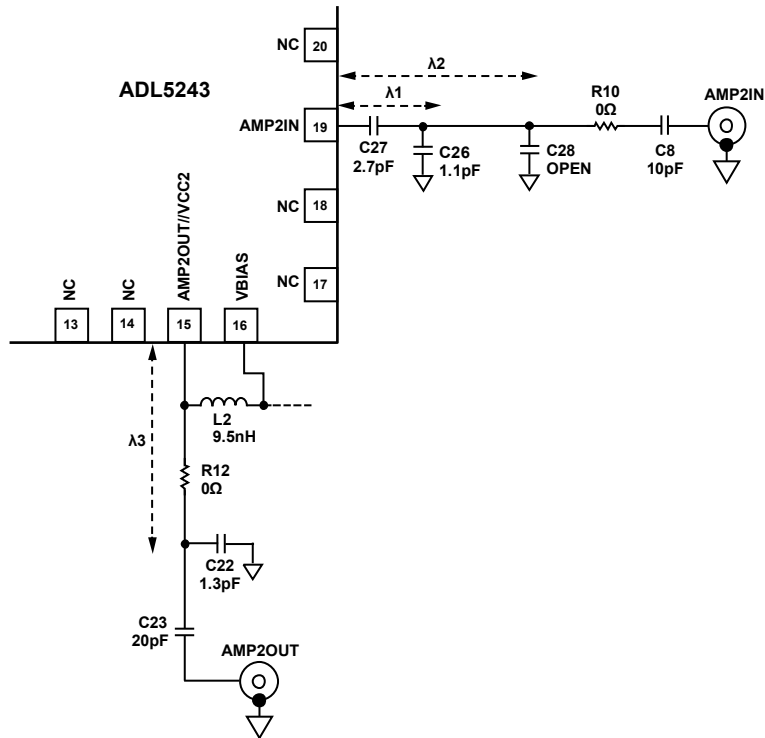


Figure 62. AMP2: Matching Circuit at 2630 MHz

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**ADL5243 LOOP PERFORMANCE**

The typical configuration of the ADL5243 is to connect in AMP1-DSA-AMP2 mode, as shown in Figure 63. Because AMP1 and DSA are broadband in nature and internally matched, only an ac-coupling capacitor is required between them. The AMP2 is externally matched for each frequency band of operation, and these matching elements should be placed between the DSA and AMP2 and at the output of AMP2. Figure 37 to Figure 45 show the performance of the ADL5243 when connected in a loop for the three primary frequency bands of operation, namely 943 MHz, 2140 MHz, and 2630 MHz.

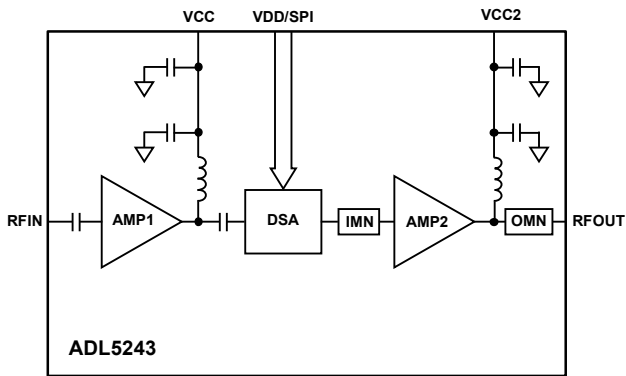


Figure 63. ADL5243 Loop Block Diagram

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**THERMAL CONSIDERATIONS**

The ADL5243 is packaged in a thermally efficient, 5 mm × 5 mm, 32-lead LFCSP. The thermal resistance from junction to air ( $\theta_{JA}$ ) is 34.8°C/W. The thermal resistance for the product was extracted assuming a standard 4-layer JEDEC board with 25 copper platter thermal vias. The thermal vias are filled with conductive copper paste, AE3030, with a thermal conductivity of 7.8 W/mk and thermal expansion as follows:  $\alpha_1$  of  $4 \times 10^{-5}/^\circ\text{C}$  and  $\alpha_2$  of  $8.6 \times 10^{-5}/^\circ\text{C}$ . The thermal resistance from junction to case ( $\theta_{JC}$ ) is 6.2°C/W, where case is the exposed pad of the lead frame package.

For the best thermal performance, it is recommended to add as many thermal vias as possible under the exposed pad of the LFCSP. The above thermal resistance numbers assume a minimum of 25 thermal vias arranged in a 5 × 5 array with a via diameter of 13 mils, via pad of 25 mils, and pitch of 25 mils. The vias are plated with copper, and the drill hole is filled with a conductive copper paste. For optimal performance, it is recommended to fill the thermal vias with a conductive paste of equivalent thermal conductivity, as mentioned above, or use an external heat sink to dissipate the heat quickly without affecting the die junction temperature. It is also recommended to extend the ground pattern as shown in Figure 64 to improve thermal efficiency.

**SOLDERING INFORMATION AND RECOMMENDED PCB LAND PATTERN**

Figure 64 shows the recommended land pattern for the ADL5243. To minimize thermal impedance, the exposed paddle on the 5 mm × 5 mm LFCSP package is soldered down to a ground plane. To improve thermal dissipation, 25 thermal vias are arranged in a 5 × 5 array under the exposed paddle. If multiple ground layers exist, they should be tied together using vias. For more information on land pattern design and layout, see the AN-772 Application Note, *A Design and Manufacturing Guide for the Lead Frame Chip Scale Package (LFCSP)*.

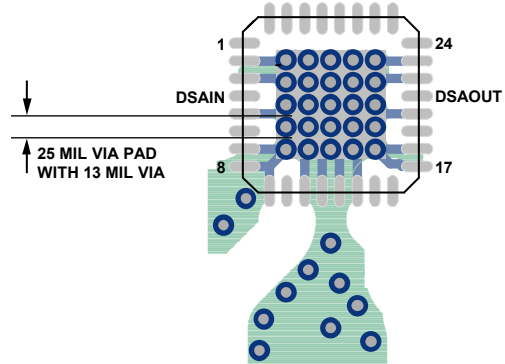


Figure 64. Recommended Land Pattern

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## EVALUATION BOARD

The schematic of the [ADL5243](#) evaluation board is shown in Figure 65. All RF traces on the evaluation board have a characteristic impedance of 50  $\Omega$  and are fabricated from Rogers3003 material. The traces are CPWG with a width of 25 mils, spacing of 20 mils, and dielectric thickness of 10 mils. The input and output to the DSA and amplifier should be ac-coupled with capacitors of appropriate value to ensure broadband performance. The bias to AMP1 is provided through a choke connected to the AMP1OUT pin and, similarly, bias to AMP2 is provided through a choke connected to the AMP2OUT pin. Bypassing capacitors are recommended on all supply lines to minimize RF coupling. The DSA and the amplifiers can be

individually biased or connected to the VDD plane through Resistors R1, R2, and R11.

When configuring the [ADL5243](#) evaluation board in the AMP1-DSA-AMP2 loop, remove Capacitors C1, C4, C5, and C8 and remove Resistor R10. Place 100 pF in place of C2, 10 pF in place of C6, and 0  $\Omega$  in place of C7 and C24. If needed, placing a shunt capacitor (1.3 pF) at the output of the DSA improves the output return loss of this loop.

On the digital signal traces, provisions for an RC filter are made to clean any potential coupled noise. In normal operation, Resistors R3 to R9 are 0  $\Omega$  and Capacitors C9 to C15 are open.

**Table 10. Evaluation Board Configurations Options**

Component	Function	Default Value
C1, C5	AC coupling caps for DSA.	C1, C5 = 100 pF
C4, C21	AC coupling capacitors for AMP1.	C4, C21 = 0.1 $\mu$ F
C13, C14, C15	Power supply bypassing capacitors for AMP1. Capacitor C15 should be closest to the device.	C13 = 1 $\mu$ F C14 = 1.2 nF C15 = 68 pF
L1	The bias for AMP1 comes through L1 when connected to a 5 V supply. L1 should be high impedance for the frequency of operation, while providing low resistance for the dc current.	L1 = 470 nH
C8	AMP2 input ac-coupling capacitor.	C8 = 10 pF
C23	AMP2 output ac-coupling capacitor.	C23 = 10 pF
C22	AMP2 shunt output tuning capacitor.	C22 = 1.0 pF at 244 mils from edge of package
C26	AMP2 shunt input tuning capacitor.	DNP
C27	AMP2 series input tuning capacitor.	C27 = 2.2 pF
C28	AMP2 shunt input tuning capacitor.	C28 = 1.8 pF at 366 mils from edge of package
C3, C25, C20	Power supply bypassing capacitors for AMP2. Capacitor C3 should be closest to the device.	C3 = 10 pF C25 = 10 nF C20 = 10 $\mu$ F
L2	The bias for AMP2 comes through L2 when connected to a 5 V supply. L2 should be high impedance for the frequency of operation, while providing low resistance for the dc current.	L2 = 9.5 nH
C17	Power supply bypassing capacitor.	C17 = 0.1 $\mu$ F
R10, R12	Placeholder for the series component for the other frequency band.	R10, R12 = 0 $\Omega$
R3, R4, R5, R6, R7, R8, R9	Digital signal filter resistors.	R3, R4, R5, R6, R7, R8, R9 = 0 $\Omega$
C9, C10, C11, C12, C16, C18, C19	Digital signal filter capacitors.	C9, C10, C11, C12, C16, C18, C19 = open
C2, C6, C7, C24	Replace with capacitors and resistors to connect the device in a loop.	C2, C6, C7, C24 = open
R1, R2, R11	Resistors to connect the supply for the amplifier and the DSA to the same VDD plane.	R1, R2 = open
S1	Switch to change between serial and parallel mode operation; connect to a supply for parallel mode and to ground for serial mode operation.	3-pin rocker
P1	Digital control.	9-pin connector

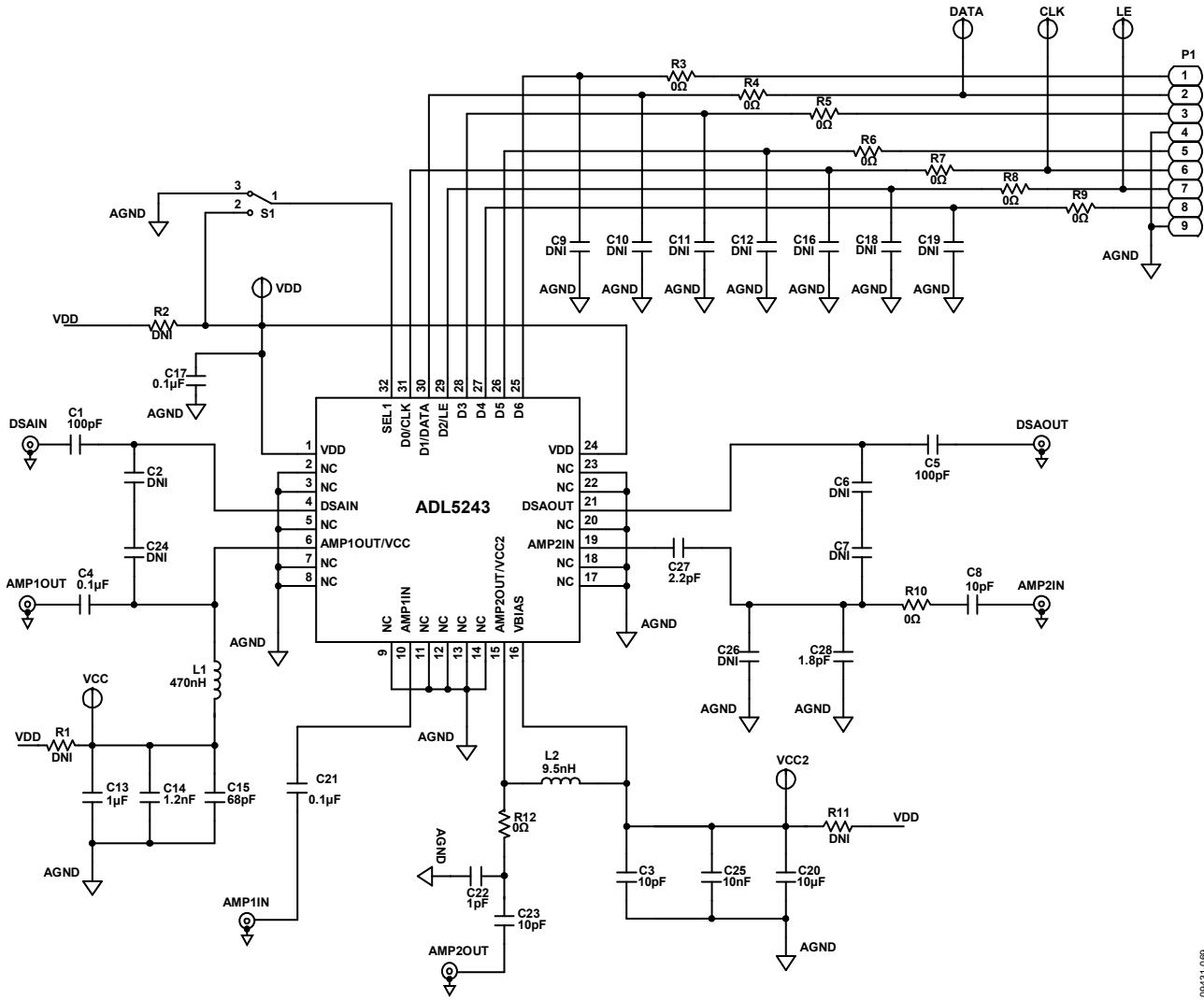


Figure 65. ADL5243 Evaluation Board

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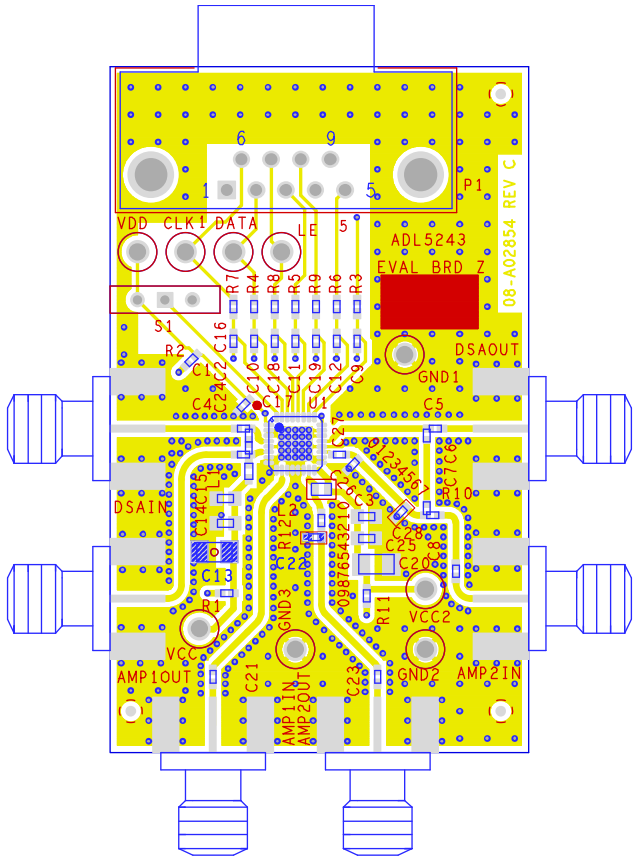


Figure 66. Evaluation Board Layout—Top

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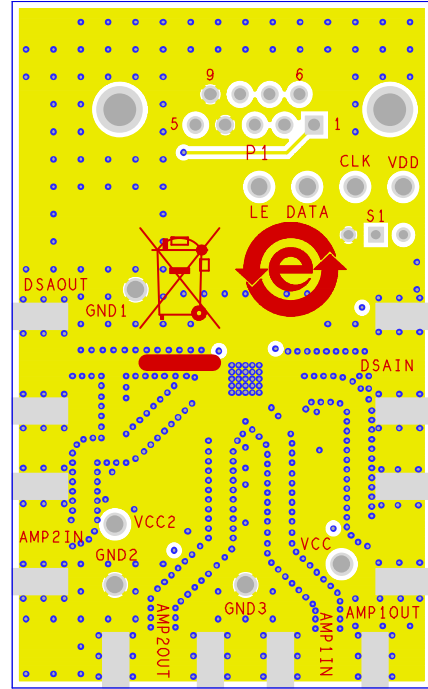
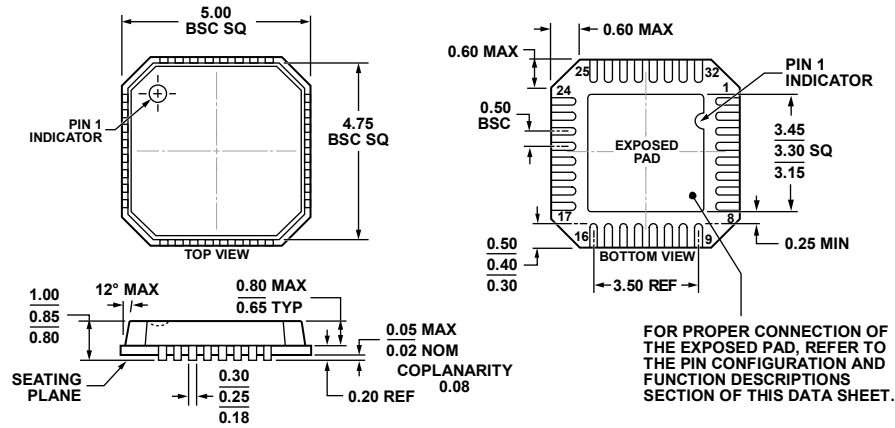


Figure 67. Evaluation Board Layout—Bottom

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OUTLINE DIMENSIONS



COMPLIANT TO JEDEC STANDARDS MO-220-VHHD-2  
 Figure 68. 32-Lead Lead Frame Chip Scale Package [LFCSP\_VQ]  
 5 mm × 5 mm Body, Very Thin Quad  
 (CP-32-3)  
 Dimensions shown in millimeters

05-85-2011-A

ORDERING GUIDE

Model <sup>1</sup>	Temperature Range	Package Description	Package Option
ADL5243ACPZ-R7	-40°C to +85°C	32-Lead Lead Frame Chip Scale Package LFCSP_VQ	CP-32-3
ADL5243-EVALZ		Evaluation Board	

<sup>1</sup> Z = RoHS Compliant Part.

**NOTES**

**NOTES**